Synchronous Buck NexFET™ Power Block

FEATURES

- Half-Bridge Power Block
- 90% system Efficiency at 25A
- Up To 40A Operation
- High Frequency Operation (Up To 1.5MHz)
- High Density – SON 5-mm × 6-mm Footprint
- Optimized for 5V Gate Drive
- Low Switching Losses
- Ultra Low Inductance Package
- RoHS Compliant
- Halogen Free
- Pb-Free Terminal Plating

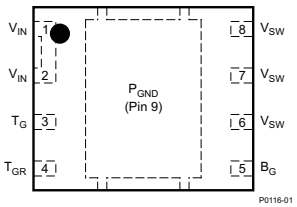
APPLICATIONS

- Synchronous Buck Converters
  - High Frequency Applications
  - High Current, Low Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters
- IMVP, VRM, and VRD Applications

DESCRIPTION

The CSD86350Q5D NexFET™ power block is an optimized design for synchronous buck applications offering high current, high efficiency, and high frequency capability in a small 5-mm × 6-mm outline. Optimized for 5V gate drive applications, this product offers a flexible solution capable of offering a high density power supply when paired with any 5V gate drive from an external controller/driver.

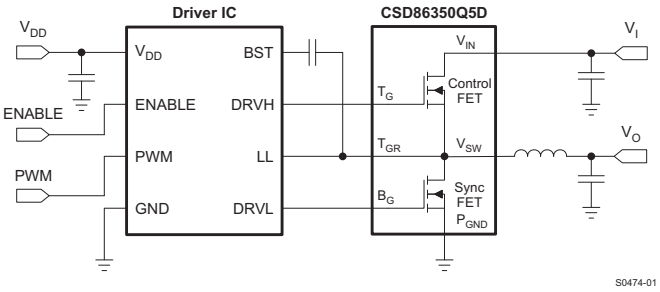
Top View



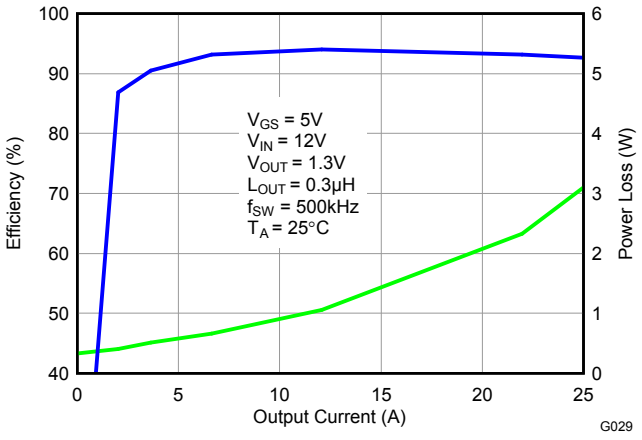
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD86350Q5D	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

TYPICAL CIRCUIT



TYPICAL POWER BLOCK EFFICIENCY and POWER LOSS



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C (unless otherwise noted) (1)

Parameter	Conditions	VALUE	UNIT
Voltage range	V_{IN} to P_{GND}	-0.8 to 25	V
	T_G to T_{GR}	-8 to 10	V
	B_G to P_{GND}	-8 to 10	V
Pulsed Current Rating, I_{DM}		120	A
Power Dissipation, P_D		13	W
Avalanche Energy E_{AS}	Sync FET, I_D = 100A, L = 0.1mH	500	mJ
	Control FET, I_D = 58A, L = 0.1mH	168	
Operating Junction and Storage Temperature Range, T_J, T_{STG}		-55 to 150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

T_A = 25° (unless otherwise noted)

Parameter	Conditions	MIN	MAX	UNIT
Gate Drive Voltage, V_{GS}		4.5	8	V
Input Supply Voltage, V_{IN}			22	V
Switching Frequency, f_{SW}	C_{BST} = 0.1µF (min)	200	1500	kHz
Operating Current			40	A
Operating Temperature, T_J			125	°C

POWER BLOCK PERFORMANCE

T_A = 25° (unless otherwise noted)

Parameter	Conditions	MIN	TYP	MAX	UNIT
Power Loss, P_{LOSS} (1)	V_{IN} = 12V, V_{GS} = 5V, V_{OUT} = 1.3V, I_{OUT} = 25A, f_{SW} = 500kHz, L_{OUT} = 0.3µH, T_J = 25ºC		2.8		W
V_{IN} Quiescent Current, I_{QVIN}	T_G to T_{GR} = 0V, B_G to P_{GND} = 0V		10		µA

(1) Measurement made with six 10µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5V driver IC.

THERMAL INFORMATION

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (Min Cu) (1)(2)			102	°C/W
	Junction to ambient thermal resistance (Max Cu) (1)(2)			50	
$R_{\theta JC}$	Junction to case thermal resistance (Top of package) (2)			20	
	Junction to case thermal resistance (P_{GND} Pin) (2)			2	

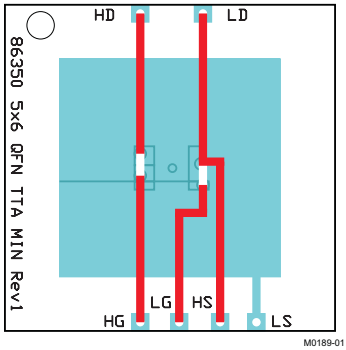
(1) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2) Cu.
(2) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2 oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS

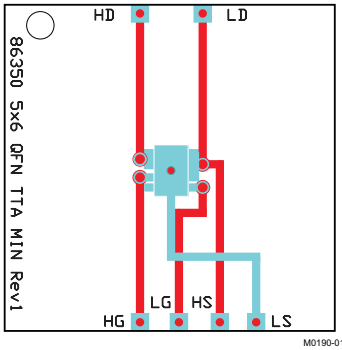
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Static Characteristics									
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_{DS} = 250µA	25			25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10 / -8			100			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250µA	0.9	1.4	2.1	0.9	1.1	1.6	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_{DS} = 20A		5	6.6		2	2.7	mΩ
		V_{GS} = 8V, I_{DS} = 20A		4.5	6		1.8	2.5	mΩ
g_{fs}	Transconductance	V_{DS} = 10V, I_{DS} = 20A		103			132		S
Dynamic Characteristics									
C_{ISS}	Input Capacitance (1)	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz		1440	1870		3080	4000	pF
C_{OSS}	Output Capacitance (1)			645	840		1550	2015	pF
C_{RSS}	Reverse Transfer Capacitance (1)			22	29		45	59	pF
R_G	Series Gate Resistance (1)			1.4	2.8		1.4	2.8	Ω
Q_g	Gate Charge Total (4.5V) (1)	V_{DS} = 12.5V, I_{DS} = 20A		8.2	10.7		19.4	25	nC
Q_{gd}	Gate Charge - Gate to Drain			1			2.5		nC
Q_{gs}	Gate Charge - Gate to Source			3.2			5.1		nC
$Q_{g(th)}$	Gate Charge at Vth			1.9			2.8		nC
Q_{OSS}	Output Charge	V_{DS} = 12V, V_{GS} = 0V		9.9			28		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_{DS} = 20A, R_G = 2Ω		8			9		ns
t_r	Rise Time			21			23		ns
$t_{d(off)}$	Turn Off Delay Time			9			24		ns
t_f	Fall Time			2.3			21		ns
Diode Characteristics									
V_{SD}	Diode Forward Voltage	I_{DS} = 20A, V_{GS} = 0V		0.85	1		0.77	1	V
Q_{rr}	Reverse Recovery Charge	V_{dd} = 12V, I_F = 20A, di/dt = 300A/µs		16			40		nC
t_{rr}	Reverse Recovery Time			22			32		ns

(1) Specified by design



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 102°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL POWER BLOCK DEVICE CHARACTERISTICS

T_J = 125°C, unless stated otherwise.

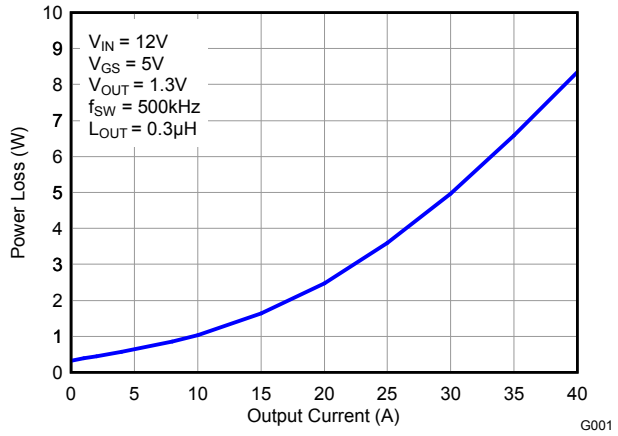


Figure 1. Power Loss vs Output Current

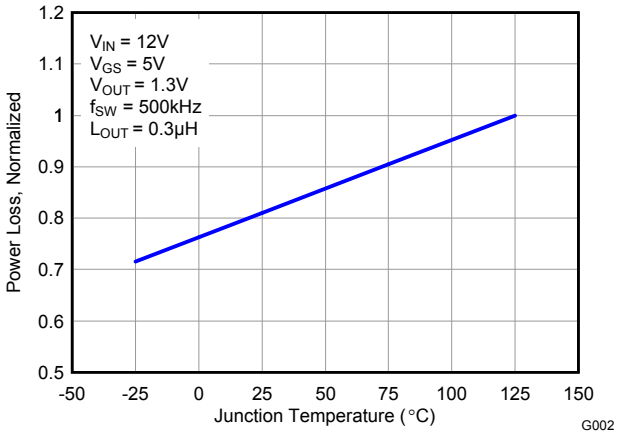


Figure 2. Power Loss vs Temperature

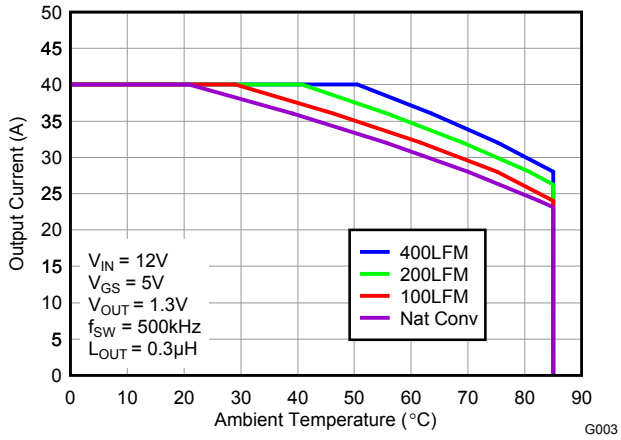


Figure 3. Safe Operating Area – PCB Vertical Mount(1)

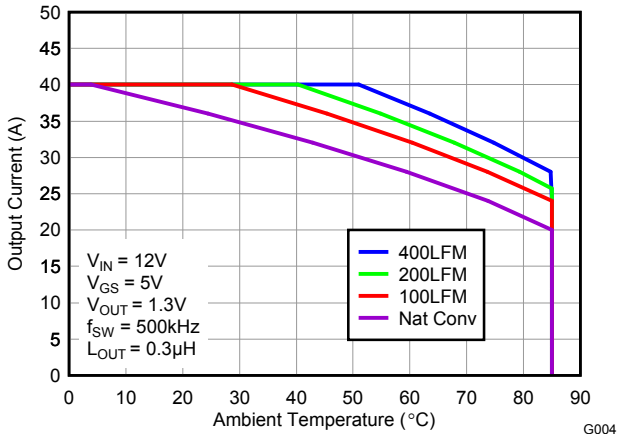


Figure 4. Safe Operating Area – PCB Horizontal Mount(1)

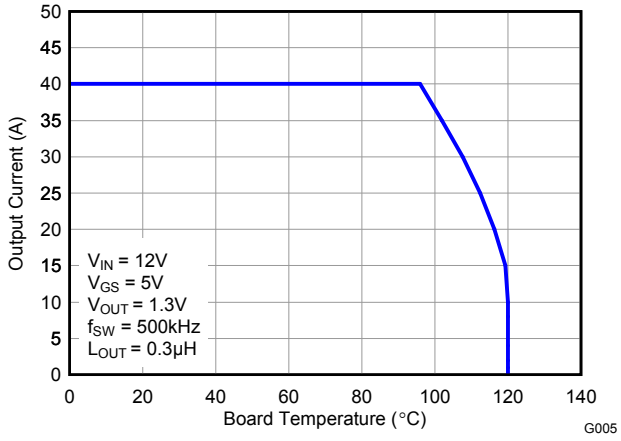


Figure 5. Typical Safe Operating Area(1)

(1) The Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0” (W) × 3.5” (L) x 0.062” (H) and 6 copper layers of 1 oz. copper thickness. See Application Section for detailed explanation.

TYPICAL POWER BLOCK DEVICE CHARACTERISTICS (continued)

T_J = 125°C, unless stated otherwise.

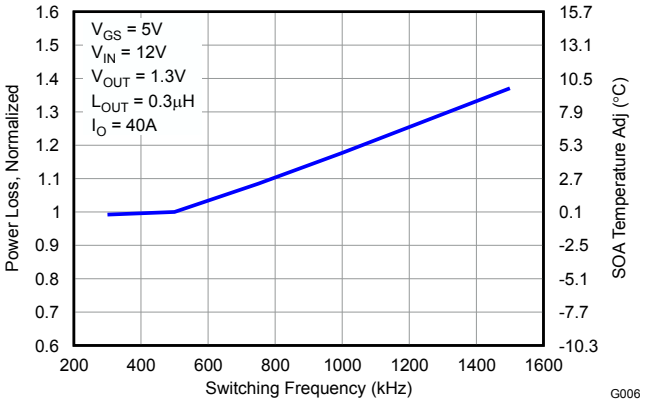


Figure 6. Normalized Power Loss vs Switching Frequency

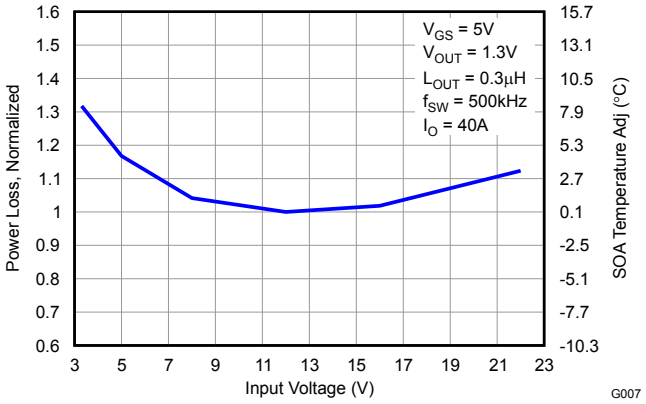


Figure 7. Normalized Power Loss vs Input Voltage

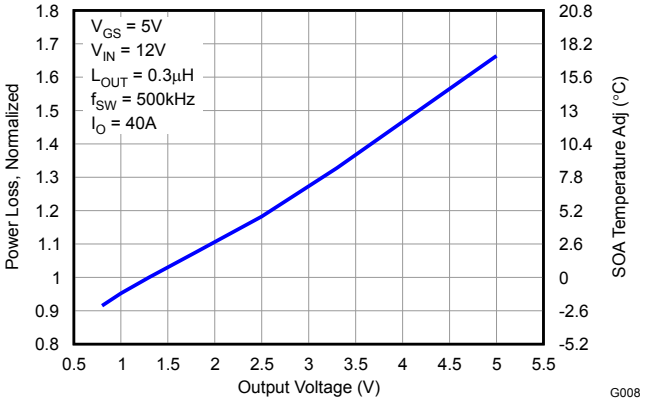


Figure 8. Normalized Power Loss vs. Output Voltage

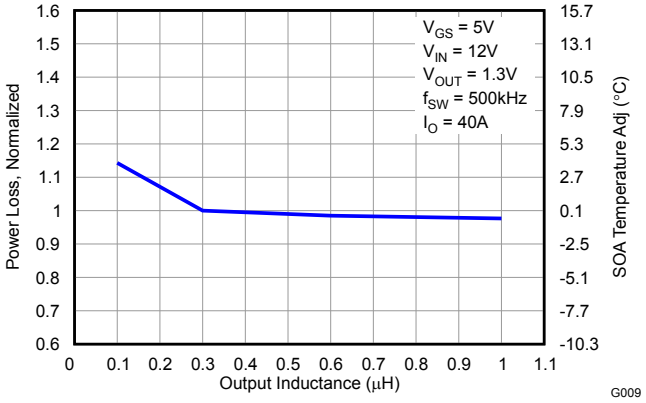


Figure 9. Normalized Power Loss vs. Output Inductance

TYPICAL POWER BLOCK MOSFET CHARACTERISTICS

T_A = 25°C, unless stated otherwise.

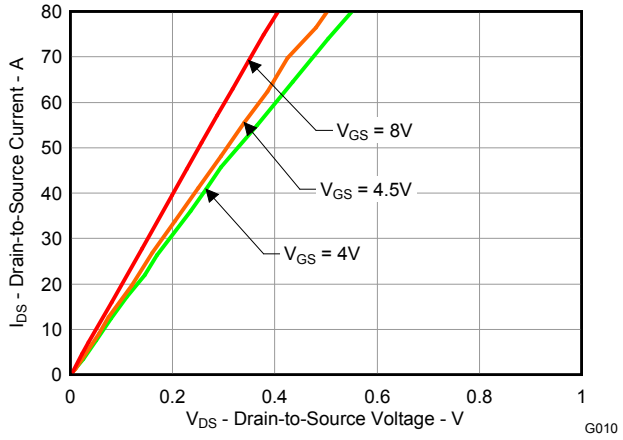


Figure 10. Control MOSFET Saturation

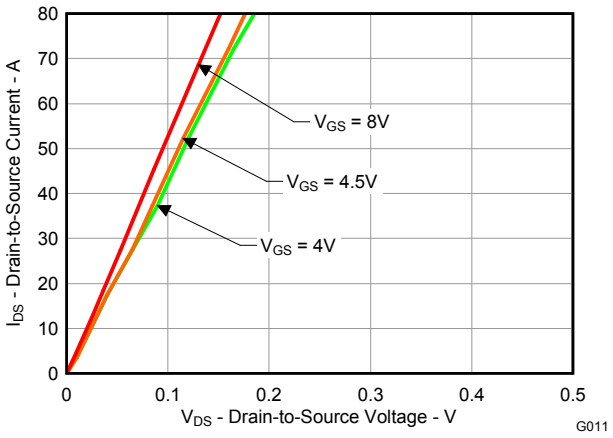


Figure 11. Sync MOSFET Saturation

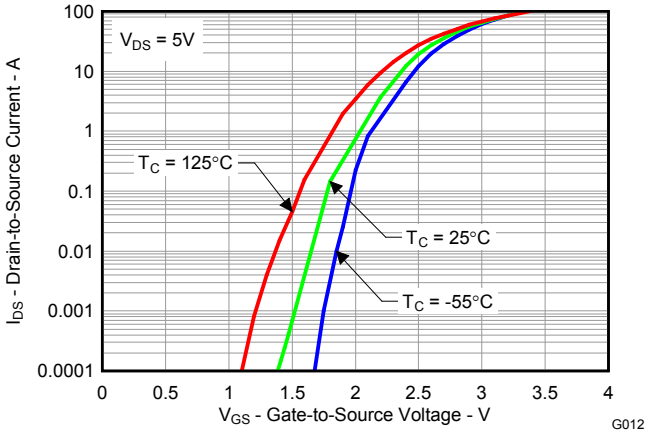


Figure 12. Control MOSFET Transfer

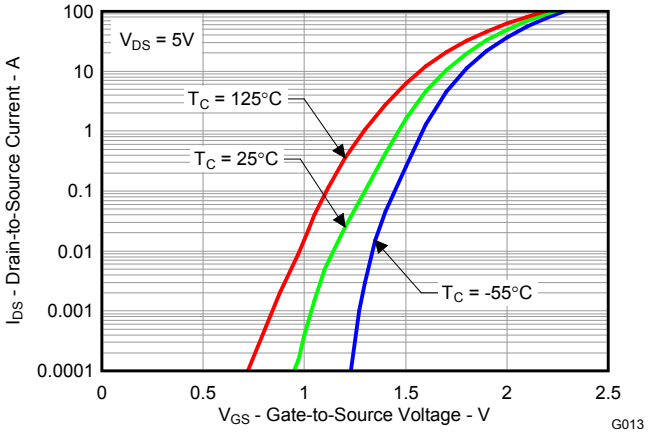


Figure 13. Sync MOSFET Transfer

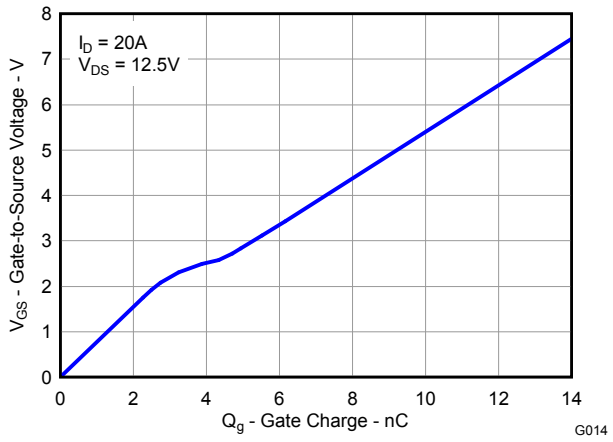


Figure 14. Control MOSFET Gate Charge

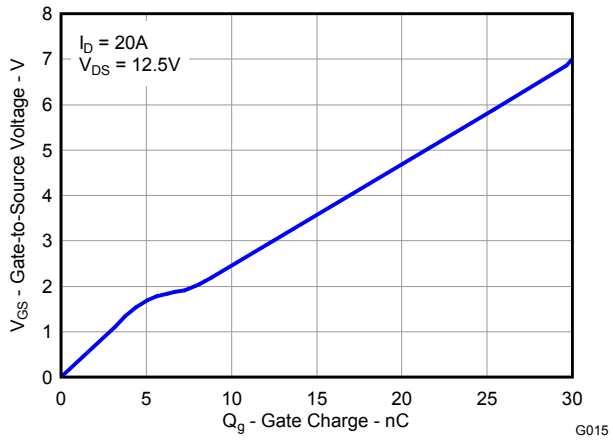


Figure 15. Sync MOSFET Gate Charge

TYPICAL POWER BLOCK MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless stated otherwise.

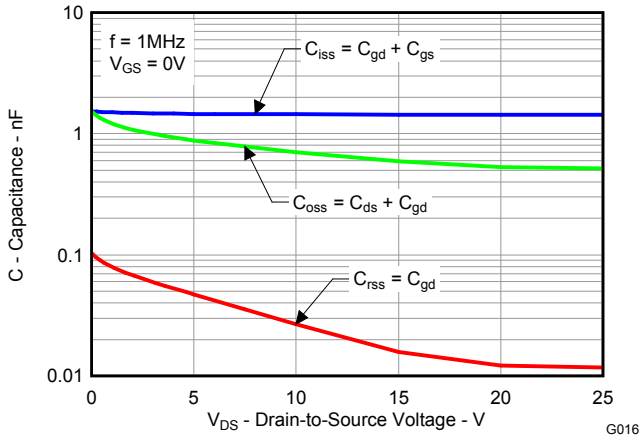


Figure 16. Control MOSFET Capacitance

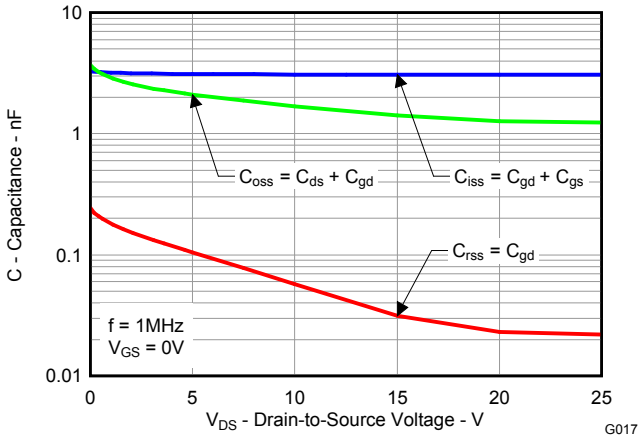


Figure 17. Sync MOSFET Capacitance

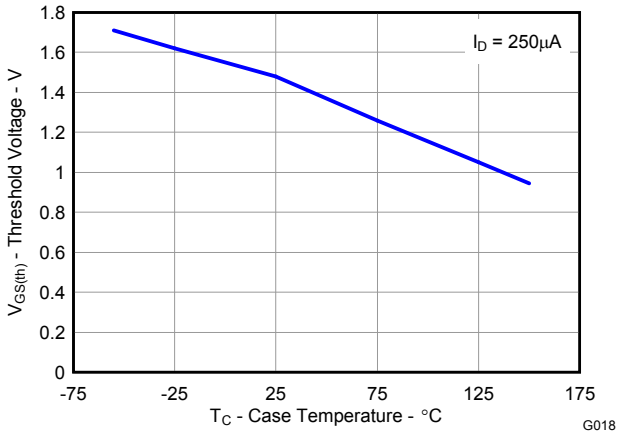


Figure 18. Control MOSFET $V_{GS(th)}$

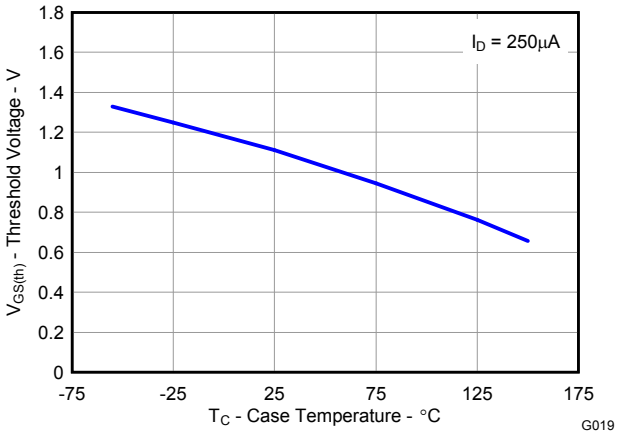


Figure 19. Sync MOSFET $V_{GS(th)}$

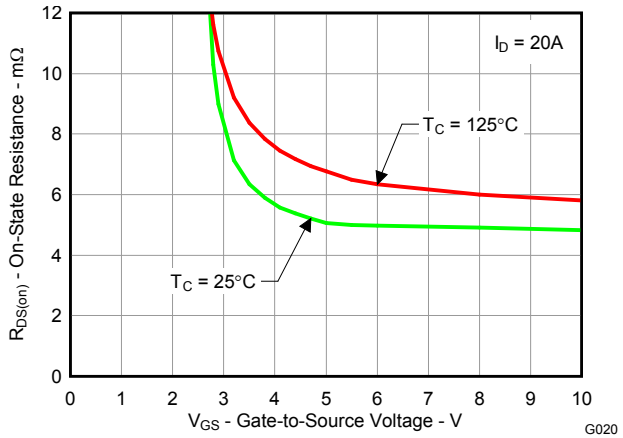


Figure 20. Control MOSFET $R_{DS(on)}$ vs V_{GS}

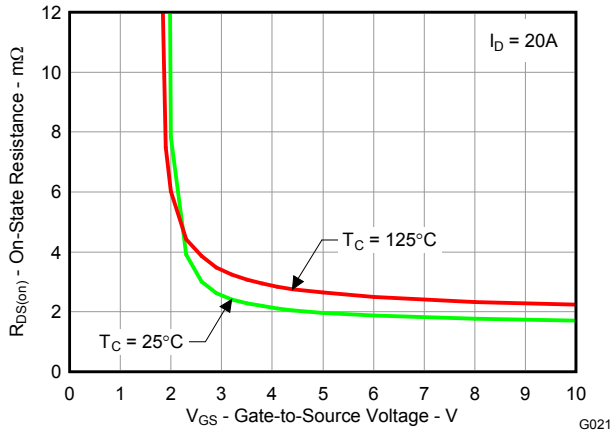


Figure 21. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

TYPICAL POWER BLOCK MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless stated otherwise.

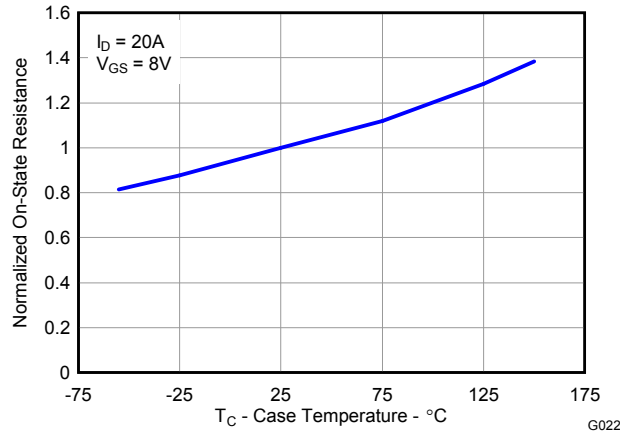


Figure 22. Control MOSFET Normalized $R_{DS(on)}$

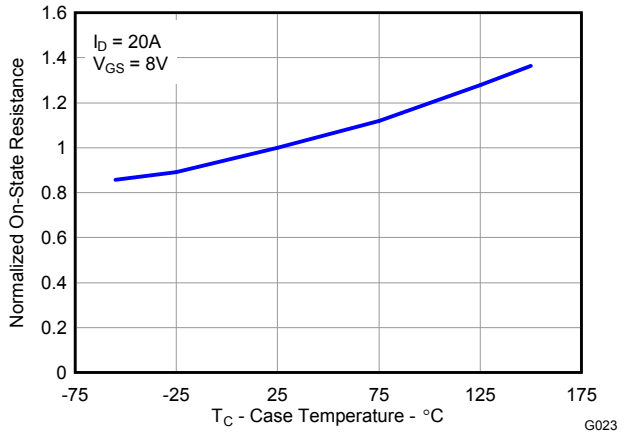


Figure 23. Sync MOSFET Normalized $R_{DS(on)}$

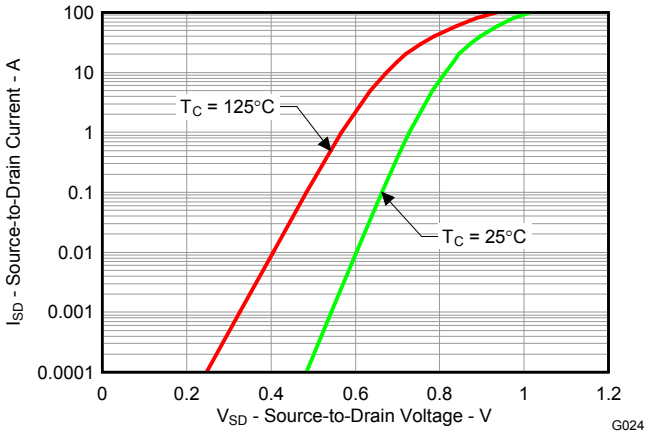


Figure 24. Control MOSFET Body Diode

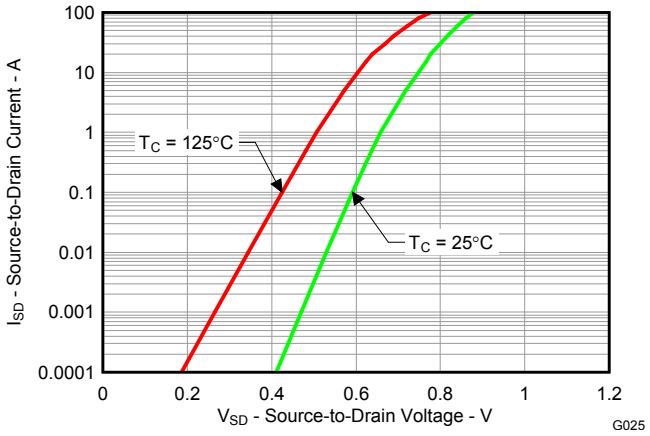


Figure 25. Sync MOSFET Body Diode

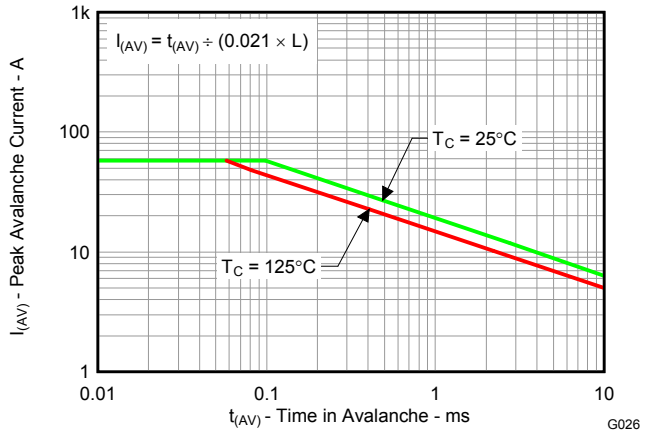


Figure 26. Control MOSFET Unclamped Inductive Switching

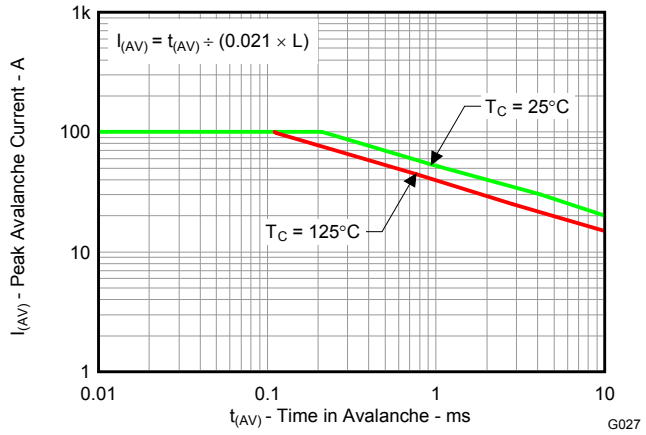


Figure 27. Sync MOSFET Unclamped Inductive Switching

APPLICATION INFORMATION

The CSD86350Q5D NexFET™ power block is an optimized design for synchronous buck applications using 5V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems centric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD86350Q5D as a function of load current. This curve is measured by configuring and running the CSD86350Q5D as it would be in the final application (see Figure 28).The measured power loss is the CSD86350Q5D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

Safe Operating Curves (SOA)

The SOA curves in the CSD86350Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 5 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4” (W) x 3.5” (L) x 0.062” (T) and 6 copper layers of 1 oz. copper thicknes

Normalized Curves

The normalized curves in the CSD86350Q5D data sheet provides guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

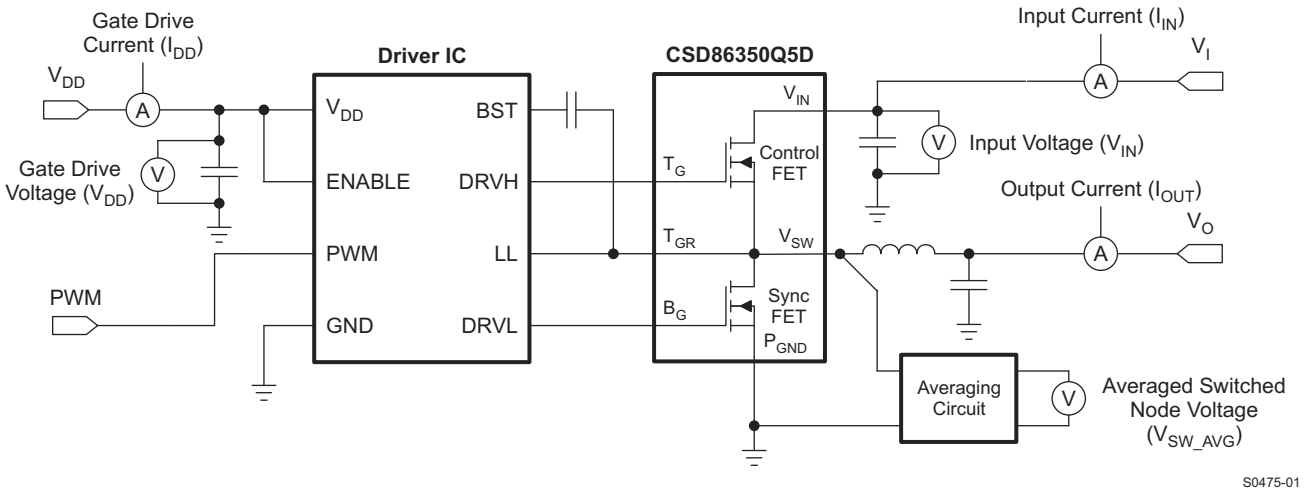


Figure 28. Typical Application

Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see Design Example). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

Design Example

Operating Conditions:

- Output Current = 25A
- Input Voltage = 7V
- Output Voltage = 1V
- Switching Frequency = 800kHz
- Inductor = 0.2µH

Calculating Power Loss

- Power Loss at 25A = 3.5W (Figure 1)
- Normalized Power Loss for input voltage ≈ 1.07 (Figure 7)
- Normalized Power Loss for output voltage ≈ 0.95 (Figure 8)
- Normalized Power Loss for switching frequency ≈ 1.11 (Figure 6)
- Normalized Power Loss for output inductor ≈ 1.07 (Figure 9)
- **Final calculated Power Loss = 3.5W x 1.07 x 0.95 x 1.11 x 1.07 ≈ 4.23W**

Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 2ºC (Figure 7)
- SOA adjustment for output voltage ≈ -1.3ºC (Figure 8)
- SOA adjustment for switching frequency ≈ 2.8ºC (Figure 6)
- SOA adjustment for output inductor ≈ 1.6ºC (Figure 9)
- **Final calculated SOA adjustment = 2 + (-1.3) + 2.8 + 1.6 ≈ 5.1ºC**

In the design example above, the estimated power loss of the CSD86350Q5D would increase to 4.23W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 5.1ºC. Figure 29 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 5.1ºC. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

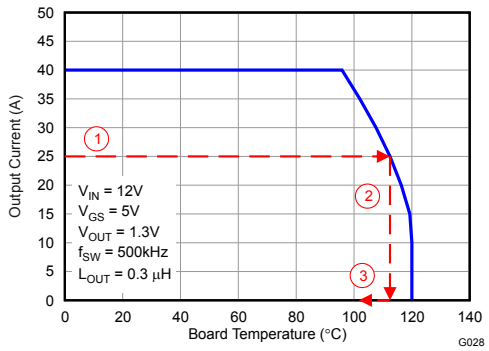


Figure 29. Power Block SOA

RECOMMENDED PCB DESIGN OVERIEW

There are two key system-level parameters that can be addressed with a proper PCB design: Electrical and Thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. A brief description on how to address each parameter is provided.

Electrical Performance

The Power Block has the ability to switch voltages at rates greater than 10kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, Driver IC, and output inductor.

- The placement of the input capacitors relative to the Power Block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 30). The example in Figure 30 uses 6x10µF ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Block, C5, C7, C19, and C8 should follow in order.
- The Driver IC should be placed relatively close to the Power Block Gate pins. T_G and B_G should connect to the outputs of the Driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the Phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the Driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the Power Block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.(1)

Thermal Performance

The Power Block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 30 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

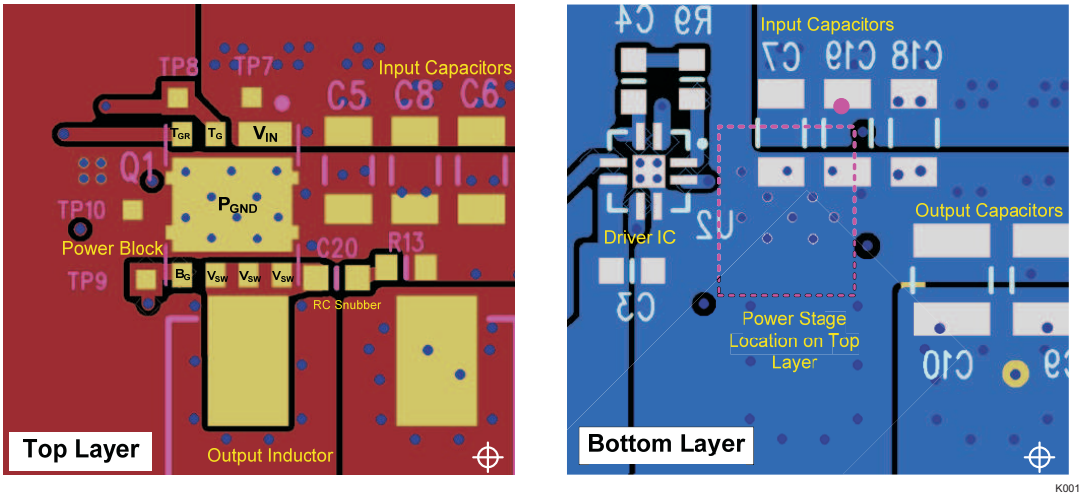
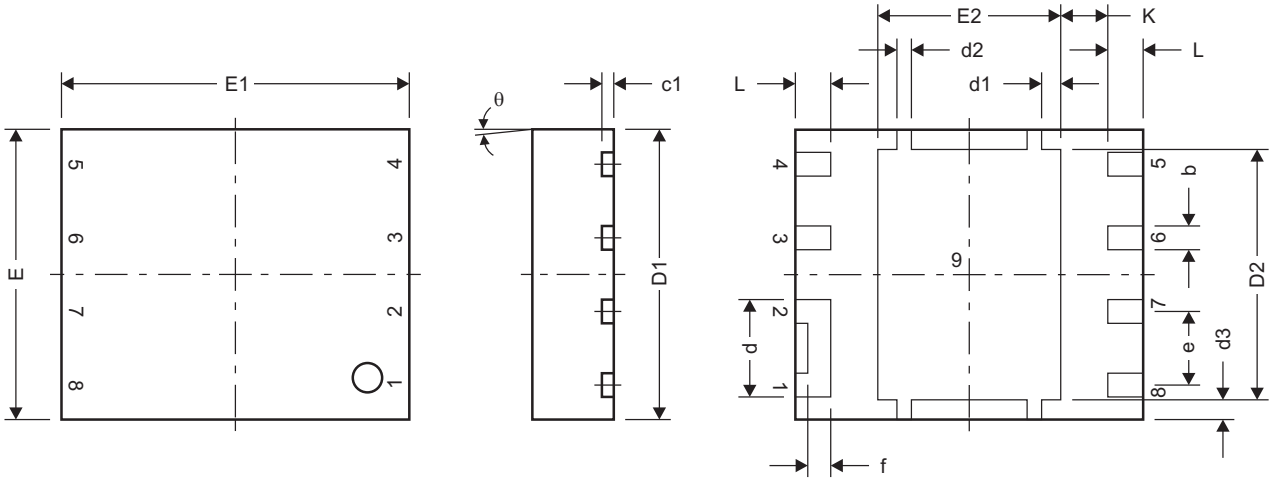


Figure 30. Recommended PCB Layout (Top Down View)

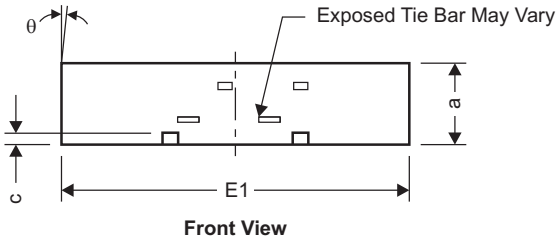
(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

MECHANICAL DATA

Q5D Package Dimensions



Top View Side View Bottom View



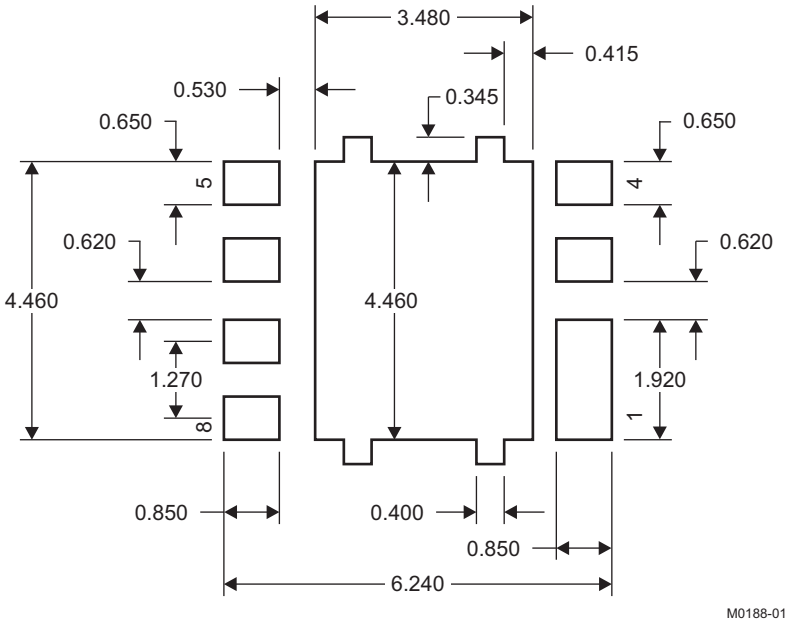
Front View

Pinout	
Position	Designation
Pin 1	V_{IN}
Pin 2	V_{IN}
Pin 3	T_G
Pin 4	T_{GR}
Pin 5	B_G
Pin 6	V_{SW}
Pin 7	V_{SW}
Pin 8	V_{SW}
Pin 9	P_{GND}

M0187-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
a	1.40	1.55	0.055	0.061
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.27 TYP		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.00	--	--	--
K	0.812		0.032	

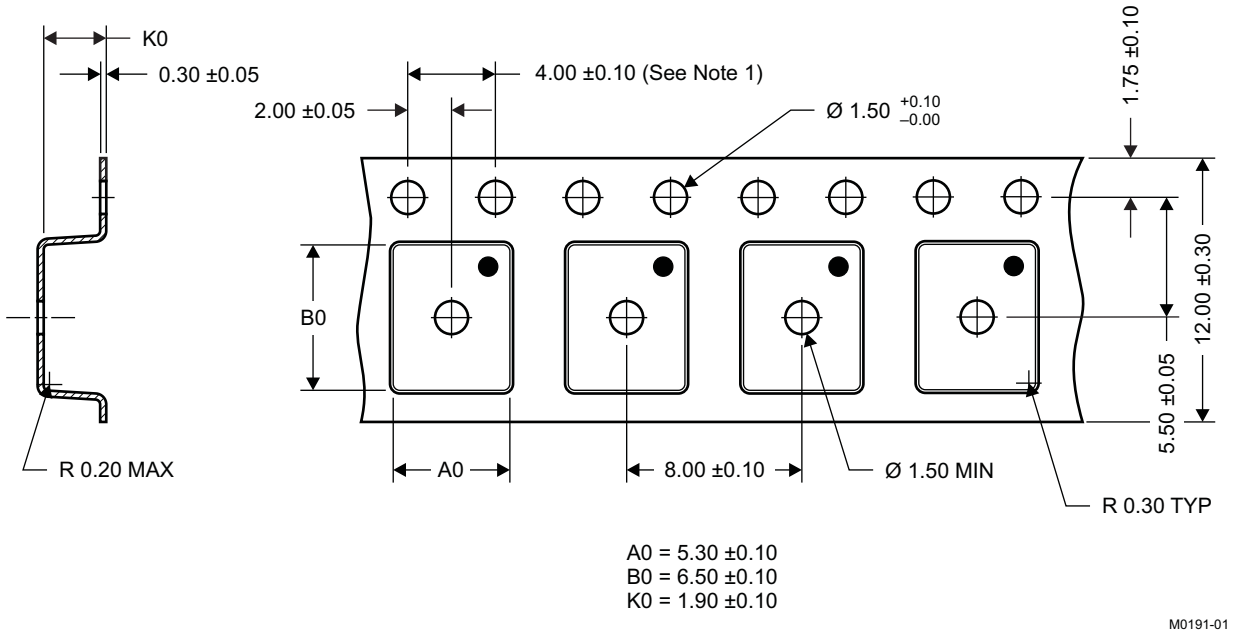
Land Pattern Recommendation



NOTE: All dimensions are in mm, unless otherwise specified.

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5D Tape and Reel Information



NOTES: 1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. Thickness: 0.30 ±0.05mm
6. MSL1 260°C (IR and convection) PbF reflow compatible

REVISION HISTORY

Changes from Original (May 2010) to Revision A	Page
• Changed graph title From: TYPICAL EFFICIENCY vs POWER LOSS To: TYPICAL POWER BLOCK EFFICIENCY and POWER LOSS	1
• Updated the Land Pattern Recommendation illustration	13

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265