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Bluetooth® 2.0 + EDR stereo audio processor

datasheet
PRELIMINARY SPECIFICATION

version 1.0 december 2010

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applications

- Bluetooth stereo headsets
- Bluetooth stereo speakers
- automotive stereo audio
- Bluetooth mini stereo soundboxes

ordering information

 OVC3860-Q56G (lead-free) 56-pin QFN

features

- highly integrated single chip Bluetooth stereo audio solution
- low power consumption
- Bluetooth V2.0 + EDR specification compliant
- Bluetooth radio with +2 dBm transmit power and -82 dBM receive sensitivity
- supports the mandatory Bluetooth compression coding/decoding scheme - Sub Band Coding (SBC) which is license-free
- integrated hi-fi stereo audio CODEC with -90 dB SNR DAC

- integrated 150 mA Lithium battery charger
- integrated switch voltage regulator
- integrated low Iq linear regulators
- supports A2DP V1.2 and AVRCP V1.4
- supports HSP V1.2 and HFP V1.5
- UART and SCCB interfaces
- low power 1.8V operation
- small footprint 56-pin QFN 7 x 7 x 0.9mm package
- RoHS compliant

key specifications

power supply:

VDD: 1.7~1.9V (1.8V typical)

V_{IO}: 1.7~3.3V V_{REG}: 2.2~4.2V

power requirements:

active: 26 mA SCO HV3: 23 mA sleep: 400 µA shutdown: 12 µA

temperature range:

operating: -10°C to 80°C (see table 5-2) storage: -45°C to 125°C (see table 5-2)

■ Bluetooth specification: version 2.0 with EDR

operating range: up to 10 meters
 modulation: n/4 DQPSK / 8DQPSK

■ transmission frequency: 2402~2480 MHz

receive sensitivity: -82 dBm @ 1% BER (typical)

maximum RF transmit power: 0 ~ +4 dBm (+2 dBm typical)

antenna impedance: 50 ohms

■ input clock: 12 MHz

package dimensions: 7 mm x 7 mm x 0.9mm

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OVC3860. The package information is shown in section 6.

table 1-1 signal description (sheet 1 of 3)

min.		I/O		
pin number	signal name	type	description	power domain
01	GPIO_A1	digital	programmable input/output terminal, LED control	Ю
02	GPIO_A0	digital	programmable input/output terminal, LED control	Ю
03	VPP	power	positive power supply of OTP ROM	OTP
04	VDD_ANA	power	positive power supply for analog circuit	core
05	VDD_RF	power	positive power supply for RF circuit	RF
06	RFA	RF	radio transmitter terminal	
07	RFB	RF	radio transmitter terminal	
08	VDD_RF	power	positive power supply for RF circuit	RF
09	VDD_LO	power	positive power supply for local oscillator circuit	
10	VDDA_RFCP	power	positive power supply for RF circuit	
11	LDO_OUT	power	linear voltage regulator output	
12	LDO_IN	power	linear voltage regulator input	
13	XTALO	analog	crystal resonator output (negative)	
14	XTALI	analog	crystal resonator output (positive)	
15	VDD_SYN	power	positive power supply for analog circuit	
16	AOM	analog	headphone common pin	
17	AOL	analog	headphone left channel output terminal	

table 1-1 signal description (sheet 2 of 3)

pin number	signal name	I/O type	description	power domain
18	VDD_AO	power	positive power supply for headphone power amplifier	
19	AOR	analog	headphone right channel output terminal	
20	VMID	analog	audio CODEC reference voltage input terminal	
21	VDDA	power	positive power supply for audio CODEC	
22	MIC	analog	microphone positive input terminal	
23	MICBIAS	analog	microphone bias output terminal	

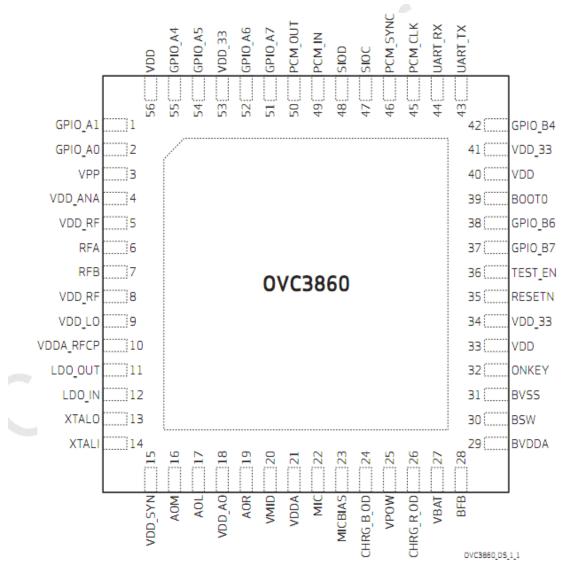
24	CHRG_B_OD	analog	charger status indicator output
25	VPOW	power	positive power supply for charger
26	CHRG_R_OD	power	charger status indicator output
27	VBAT	power	charger output to battery terminal
28	BFB	power	switch regulator feedback input terminal
29	BVDDA	power	positive power supply for Buck
30	BSW	power	switch regulator output terminal
31	BVSS	power	exposed pad as ground
32	ONKEY	digital	soft power ON/OFF control terminal
33	VDD	power	positive power supply for digital core
34	VDD_33	power	positive power supply for digital I/O
35	RESETN	digital	chip reset enable (active low)
36	TEST_EN	digital	enable test mode (connect to ground)
37	GPIO_B7	digital	programmable I/O terminal
38	GPIO_B6	digital	programmable I/O terminal
39	воото	digital	select boot position
40	VDD	power	positive power supply for digital core

table 1-1 signal description (sheet 3 of 3)

pin number	signal name	I/O type	description	power domain
54	GPIO_A5	digital	programmable I/O terminal	
55	GPIO_A4	digital	programmable I/O terminal	
56	VDD	power	positive power supply for digital core	

figure 1-1 pin diagram

41	VDD_33	power	positive power supply for digital I/O
42	GPIO_B4	digital	programmable I/O terminal
43	UART_TX	digital	UART interface data output terminal
44	UART_RX	digital	UART interface data input terminal
45	PCM_CLK	digital	PCM interface clock
46	PCM_SYNC	digital	PCM interface sync
47	SIOC	digital	SCCB interface clock output terminal
48	SIOD	digital	SCCB interface data terminal
49	PCM_IN	digital	PCM interface data in
50	PCM_OUT	digital	PCM interface data out
51	GPIO_A7	digital	programmable I/O terminal
52	GPIO_A6	digital	programmable I/O terminal
53	VDD_33	power	positive power supply for digital I/O
	·		



2 system level description

2.1 overview

The OVC3860 is a highly integrated, low power single-chip Bluetooth® RF transceiver and baseband processor for ultra low cost Bluetooth stereo audio solutions.

The OVC3860 features a 2.4GHz ISM RF transceiver, Bluetooth V2.0+EDR baseband, high-quality 20-bit stereo audio CODEC and a complete on-chip power management unit including switch regulator, Lithium ion/polymer battery charger, and low Iq linear regulators.

A configurable Bluetooth stack is integrated with profiles and applications including A2DP V1.2, AVRCP V1.4, HSP V1.2 and HPF V1.5. Incorporated with an on-chip SBC decoder, the OVC3860 is fully compliant with the Bluetooth 2.0+EDR specification. It fulfills all Bluetooth stereo audio and voice communication functions.

2.2 key features

2.2.1 general

- · cost effective, low power consumption, single-chip solution for Bluetooth stereo audio applications
- · Bluetooth V2.0 + EDR specification compliant fully integrated RF and baseband processor

2.2.2 radio

- · Bluetooth V2.0 + EDR specification compliant system in 2.4GHz ISM band
- typical +2 dbm transmit power
- · typical -83 dBm receive sensitivity
- · supports Class 2 and Class 3 without the need of an external power amplifier
- · up to 10 meters communication range

2.2.3 baseband processor

- · on-chip low power, high performance, 32-bit RISC processor
- · 2Mb internal ROM and 48kB internal RAM
- fully integrated Bluetooth baseband logic for FEC, HEC, access code correlation, CRC, demodulation, encryption bit stream generation, whitening
- fully supports Bluetooth V2.0 + EDR features including AFH and enhanced data rate up to 3 Mbps
- · supports CVSD transcoder for voice over air

2.2.4 synthesizer

- · fully integrated synthesizer
- 12MHz crystal compatible

2.2.5 digital nterfaces

- · integrated high speed UART interface for system debugging
- · SCCB interface for external EEPROM to store device configuration data

OVC3860

Bluetooth* 2.0 + FDR stereo audio processor

2.2.6 stereo audio CODEC

- integrated high fidelity audio CODEC with SNR > 90dB playback
- on-chip 20-bit stereo audio digital-to-analog converter (DAC)
- on-chip 16-bit mono voice analog-to-digital converter (ADC)
- integrated headphone amplifier in 40mW @ 32Ω supporting capacitor-less output
- one-channel microphone input with microphone driver

2.2.7 power

- low power 1.8V core operation and 1.8V to 3.3V I/O
- on-chip high efficiency switched mode regulator up to 96%, from 2.7V to 4.5V input and adjustable 1.8/2.1/2.3V output
- on-chip, fully-functional, single-cell Lithium ion/polymer battery charger with programmable charging current between 10 to 150mA with ±7% accuracy
- power-on reset programmable battery low voltage detection
- supports standard sniff/hold power save mode and OmniVision extended modes

2.2.8 Bluetooth stack

- on-chip Bluetooth stack allows full-speed data transfer and Piconet support
- on-chip A2DP V1.2 and AVRCP V1.4 profiles with hardware SBC decoder enables audio stream over Bluetooth and remote control
- on-chip HFP V1.5 and HSP V1.2 profiles

2.2.9 package

small footprint 56-pin QFN 7 x 7 x 0.9mm, 0.4mm pitch

2.3 architecture

figure 2-1 functional block diagram

