

# TLC1078, TLC1078Y, TLC1079, TLC1079Y LinCMOS™ $\mu$ POWER PRECISION OPERATIONAL AMPLIFIERS

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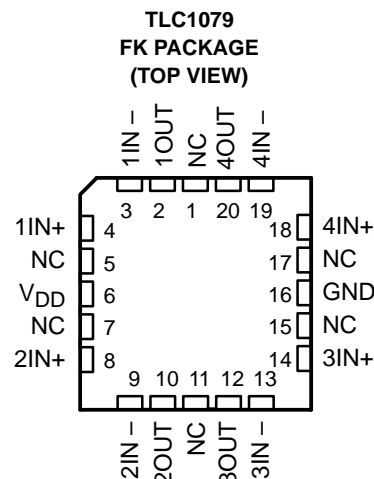
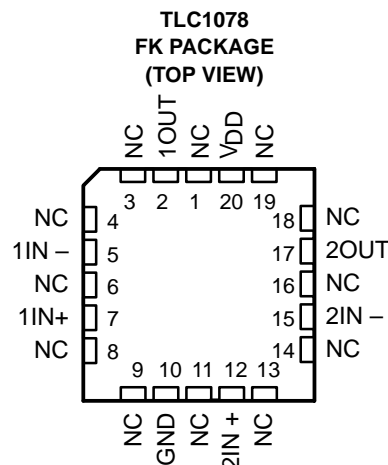
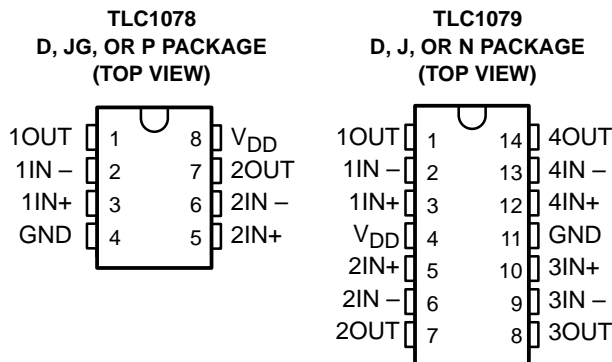
- Power Dissipation as Low as 10  $\mu$ W Typ Per Amplifier
- Operates on a Single Silver-Oxide Watch Battery,  $V_{DD} = 1.4$  V Min
- $V_{IO} \dots 450 \mu\text{V}/850 \mu\text{V}$  Max in DIP and Small-Outline Package (TLC1078/79)
- Input Offset Voltage Drift  $\dots 0.1 \mu\text{V}/\text{Month}$  Typ, Including the First 30 Days
- High-impedance LinCMOS™ Inputs  
 $I_{IB} = 0.6$  pA Typ
- High Open-Loop Gain  $\dots 800000$  Typ
- Output Drive Capability  $> 20$  mA
- Slew Rate  $\dots 47$  V/ms Typ
- Common-Mode Input Voltage Range Extends Below the Negative Rail
- Output Voltage Range Includes Negative Rail
- On-Chip ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel

## description

The TLC107x operational amplifiers offer ultra-low offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150- $\mu$ W power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC107xC is an ideal solution for low-voltage battery-operated systems. The 20-mA output drive capability means that the TLC107x can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

Since this device is functionally compatible as well as pin compatible with the TLC27L2/4 and TLC27L7/9, the TLC107x easily upgrades existing designs that can benefit from its improved performance.



NC – No internal connection



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# TLC1078, TLC1078Y, TLC1079, TLC1079Y

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### description (continued)

The TLC107x incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-PRF-38535, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC107x design also inhibits latch-up of the device inputs and outputs even with surge currents as large 100 mA.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C. The wide range of packaging options includes small-outline and chip-carrier versions for high-density system applications.

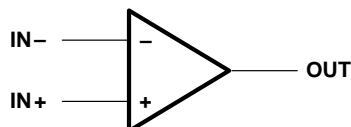
#### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES						CHIP FORM‡ (Y)
	SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	
0°C to 70°C	TLC1078CD TLC1079CD	—	—	—	TLC1079CN	TLC1078CP	TLC1078Y TLC1079Y
–40°C to 85°C	TLC1078ID TLC1079ID	—	—	—	TLC1079IN	TLC1078IP	—
–55°C to 125°C	TLC1078MD TLC1079MD	TLC1078MFK TLC1079MFK	TLC1079MJ	TLC1078MJG	TLC1079MN	TLC1078MP	—

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1078CDR).

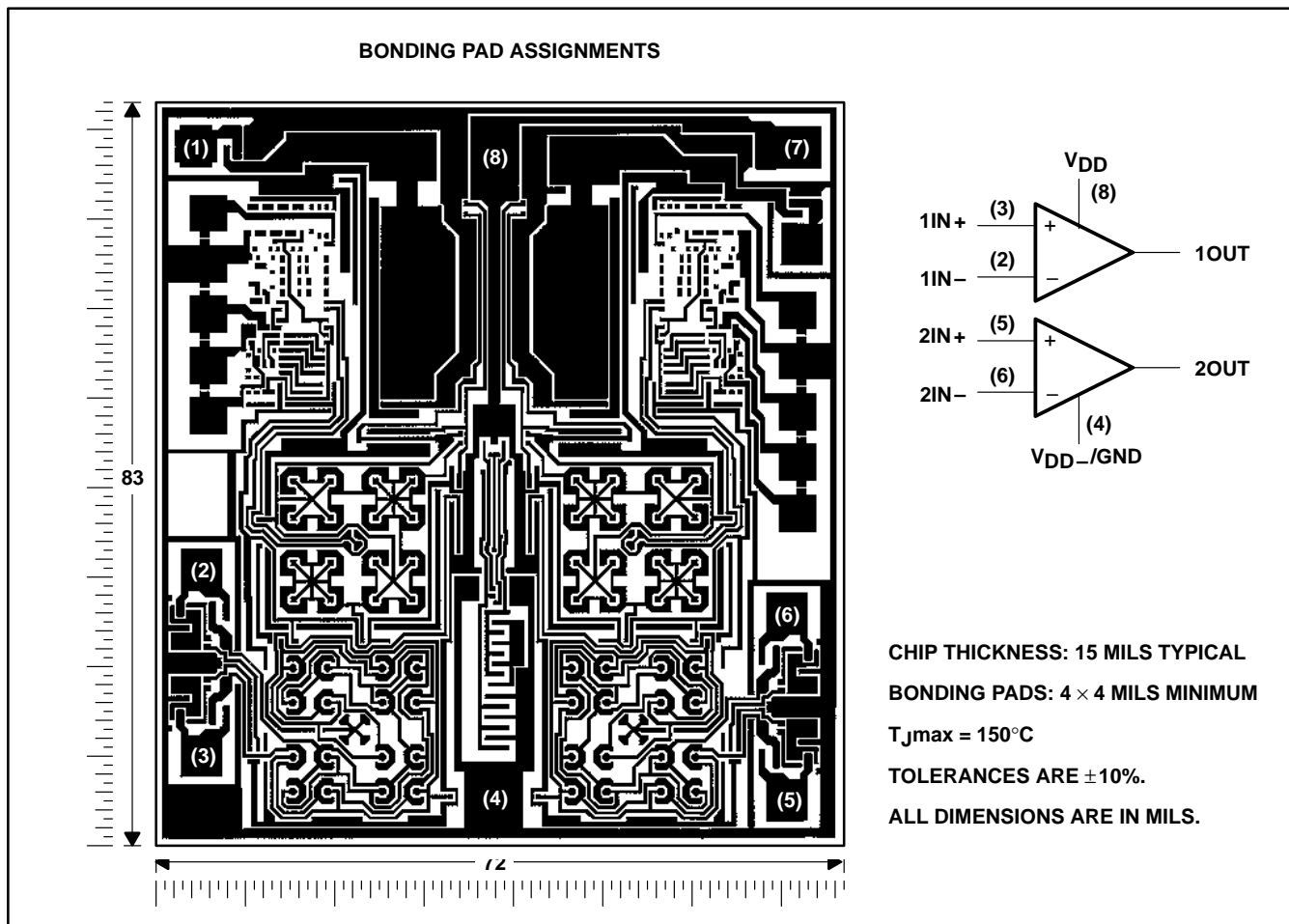
‡ Chip forms are tested 25°C only.

### symbol (each amplifier)



### TLC1087Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC1078C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.

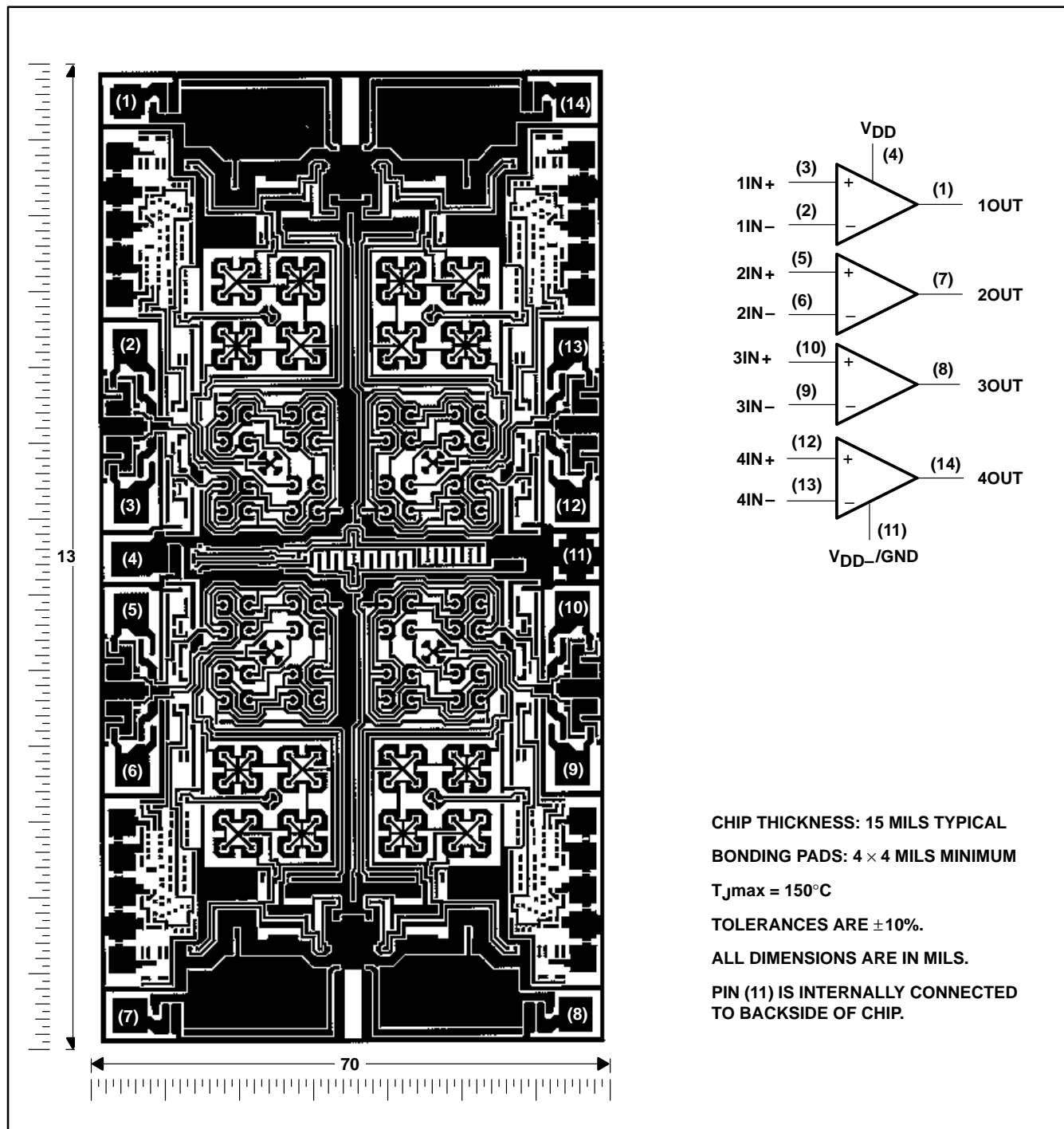


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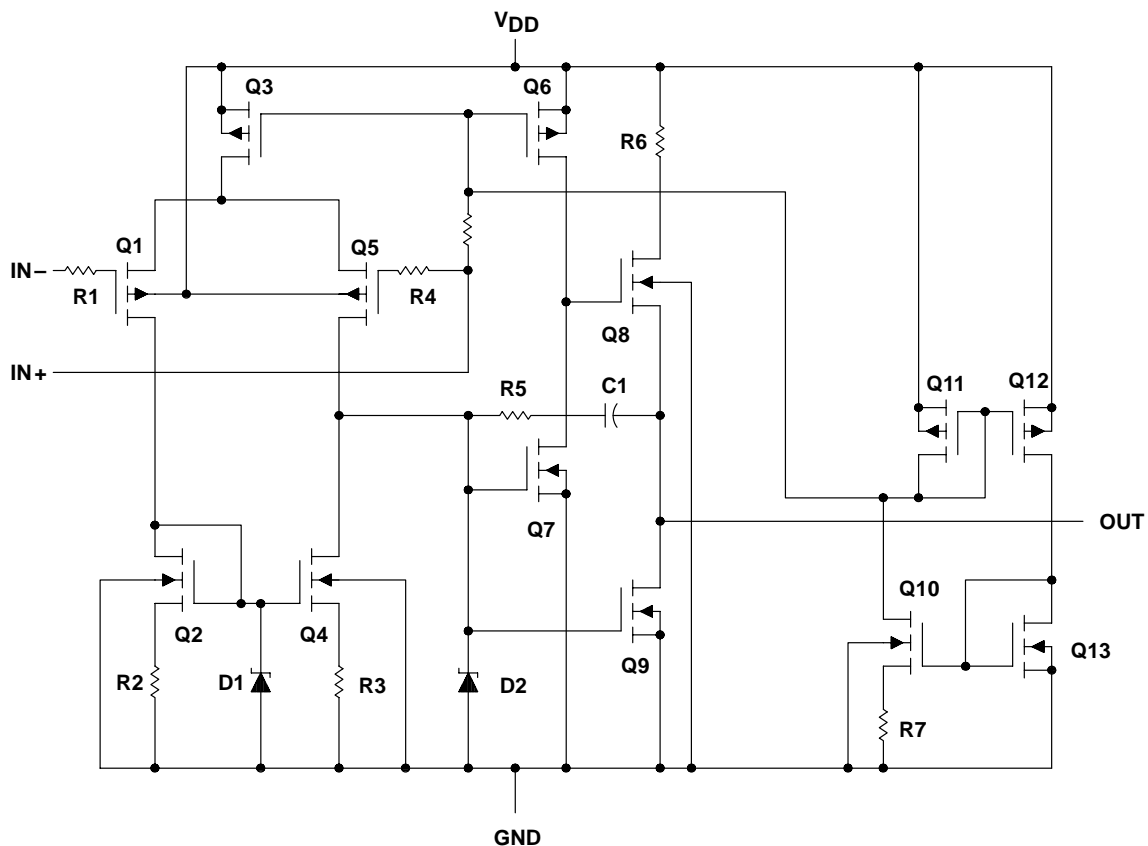
**TLC1079Y chip information**

This chip, when properly assembled, display characteristics similar to the TLC1079C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.



CHIP THICKNESS: 15 MILS TYPICAL  
 BONDING PADS: 4 × 4 MILS MINIMUM  
 $T_{jmax} = 150^{\circ}C$   
 TOLERANCES ARE  $\pm 10\%$ .  
 ALL DIMENSIONS ARE IN MILS.  
 PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT		
COMPONENT	TLC1078	TLC1079
Transistors	38	76
Resistors	16	32
Diodes	12	24
Capacitors	2	4

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{DD}$ (see Note 1)	18 V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm V_{DD}$
Input voltage range, $V_I$ (any input)	-0.3 V to $V_{DD}$
Input current, $I_I$ (each input)	$\pm 5$ mA
Output current, $I_O$ (each output)	$\pm 30$ mA
Total current into $V_{DD}$ (see Note 3)	45 mA
Duration of short-circuit at (or below) $T_A = 25^\circ\text{C}$ (see Note 3)	unlimited
Continuous total power dissipation	see Dissipation Rating Table
Operating free-air temperature range, $T_A$ : C suffix	0°C to 70°C
I suffix	-40°C to 85°C
M suffix	-55°C to 125°C
Storage temperature range	-65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.  
 2. Differential voltages are at  $IN+$  with respect to  $IN-$ .  
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings are not exceeded.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D-14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

**recommended operating conditions**

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD}$	1.4	16	3	16	4	16	V
Common-mode input voltage, $V_{IC}$	$V_{DD} = 5$ V		-0.2	4	-0.2	4	V
	$V_{DD} = 10$ V		-0.2	9	-0.2	9	
Operating free-air temperature, $T_A$	0	70	-40	85	-55	125	°C



**electrical characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TLC1078C						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 1.4 V, R <sub>S</sub> = 50 Ω, V <sub>IC</sub> = 0, R <sub>I</sub> = 1 MΩ	25°C	160	450		180	600	μV	
		Full range		800		950			
α <sub>VIO</sub> Temperature coefficient of input offset voltage		25°C to 70°C	1.1			1			μV/°C
I <sub>IO</sub> Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.1	60		0.1	60	pA	
		70°C	7	300		7	300		
I <sub>IB</sub> Input bias current (see Note 4)			25°C	0.6	60		0.7	60	pA
		70°C	40	600		50	600		
V <sub>ICR</sub> Common-mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2	V	
		Full range	-0.2 to 3.5			-0.2 to 8.5		V	
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 1 MΩ	25°C	3.2	4.1		8.2	8.9	V	
		0°C	3.2	4.1		8.2	8.9		
		70°C	3.2	4.2		8.2	8.9		
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C	0	25		0	25	mV	
		0°C	0	25		0	25		
		70°C	0	25		0	25		
A <sub>VD</sub> Large-signal differential voltage amplification	R <sub>L</sub> = 1 MΩ, See Note 6	25°C	250	525		500	850	V/mV	
		0°C	250	680		500	1010		
		70°C	200	380		350	660		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	70	95		75	97	dB	
		0°C	70	95		75	97		
		70°C	70	95		75	97		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 1.4 V	25°C	75	98		75	98	dB	
		0°C	75	98		75	98		
		70°C	75	98		75	98		
I <sub>DD</sub> Supply current (two amplifiers)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C	20	34		29	46	μA	
		0°C	24	42		36	66		
		70°C	16	28		22	40		

† Full range is 0°C to 70°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.  
5. This range also applies to each input individually.  
6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.

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**electrical characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC1079C						UNIT
			$V_{DD} = 5\text{ V}$			$V_{DD} = 10\text{ V}$			
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 1.4\text{ V}, V_{IC} = 0,$ $R_S = 50\ \Omega, R_I = 1\text{ M}\Omega$	25°C	190	850	200	1150	$\mu\text{V}$		
Full range		1200			1500				
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25°C to 70°C	1.1			1		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$ Input offset current (see Note 4)	$V_O = V_{DD}/2,$ $V_{IC} = V_{DD}/2$	25°C	0.1	60	0.1	60	$\text{pA}$		
		70°C	7	300	7	300			
$I_{IB}$ Input bias current (see Note 4)		25°C	0.6	60	0.7	60	$\text{pA}$		
		70°C	40	600	50	600			
$V_{ICR}$ Common mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2	-0.2 to 9	-0.3 to 9.2	V		
		Full range	-0.2 to 3.5		-0.2 to 8.5		V		
$V_{OH}$ High-level output voltage	$V_{ID} = 100\text{ mV},$ $R_L = 1\text{ M}\Omega$	25°C	3.2	4.1	8.2	8.9	V		
		0°C	3.2	4.1	8.2	8.9			
		70°C	3.2	4.2	8.2	8.9			
$V_{OL}$ Low-level output voltage	$V_{ID} = -100\text{ mV},$ $I_{OL} = 0$	25°C	0	25	0	25	mV		
		0°C	0	25	0	25			
		70°C	0	25	0	25			
$A_{VD}$ Large-signal differential voltage amplification	$R_L = 1\text{ M}\Omega,$ See Note 6	25°C	250	525	500	850	V/mV		
		0°C	250	700	500	1010			
		70°C	200	380	350	660			
CMRR Common mode rejection ratio	$V_{IC} = V_{ICRmin}$	25°C	70	95	75	97	dB		
		0°C	70	95	75	97			
		70°C	70	95	75	97			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 5\text{ V to }10\text{ V},$ $V_O = 1.4\text{ V}$	25°C	75	98	75	98	dB		
		0°C	75	98	75	98			
		70°C	75	98	75	98			
$I_{DD}$ Supply current (four amplifiers)	$V_O = V_{DD}/2,$ $V_{IC} = V_{DD}/2,$ No load	25°C	40	68	57	92	$\mu\text{A}$		
		0°C	48	84	72	132			
		70°C	31	56	44	80			

† Full range is 0°C to 70°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.  
5. This range also applies to each input individually.  
6. At  $V_{DD} = 5\text{ V}, V_O = 0.25\text{ V to }2\text{ V};$  at  $V_{DD} = 10\text{ V}, V_O = 1\text{ V to }6\text{ V}.$





operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TLC1078C						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	R <sub>L</sub> = 1 M $\Omega$ , C <sub>L</sub> = 20 pF, V <sub>I(PP)</sub> = 1 V, See Figure 1	25°C	32			47			V/ms
		0°C	35			51			
		70°C	27			38			
V <sub>n</sub> Equivalent input noise voltage	f = 1 kHz, R <sub>S</sub> = 20 $\Omega$	25°C	68			68			nV/ $\sqrt{\text{Hz}}$
B <sub>1</sub> Unity-gain bandwidth	C <sub>L</sub> = 20 pF, See Figure 2	25°C	85			110			kHz
		0°C	100			125			
		70°C	65			90			
$\phi_m$ Phase margin at unity gain	C <sub>L</sub> = 20 pF, See Figure 2	25°C	34°			38°			
		0°C	36°			40°			
		70°C	30°			34°			

operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TLC1079C						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	R <sub>L</sub> = 1 M $\Omega$ , C <sub>L</sub> = 20 pF, V <sub>I(PP)</sub> = 1 V, See Figure 1	25°C	32			47			V/ms
		0°C	35			51			
		70°C	27			38			
V <sub>n</sub> Equivalent input noise voltage	f = 1 kHz, R <sub>S</sub> = 20 $\Omega$	25°C	68			68			nV/ $\sqrt{\text{Hz}}$
B <sub>1</sub> Unity-gain bandwidth	C <sub>L</sub> = 20 pF, See Figure 2	25°C	85			110			kHz
		0°C	100			125			
		70°C	65			90			
$\phi_m$ Phase margin at unity gain	C <sub>L</sub> = 20 pF, See Figure 2	25°C	34°			38°			
		0°C	36°			40°			
		70°C	30°			34°			

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**electrical characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TLC1078I						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>O</sub> = 1.4 V, R <sub>S</sub> = 50 Ω, V <sub>IC</sub> = 0, R <sub>I</sub> = 1 MΩ	25°C	160	450	180	600	μV	
α <sub>VIO</sub>	Temperature coefficient of input offset voltage		Full range	950		1100		μV/°C	
I <sub>IO</sub>	Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.1	60	0.1	60	pA	
I <sub>IB</sub>	Input bias current (see Note 4)		85°C	24	1000	26	1000	pA	
V <sub>ICR</sub>	Common-mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2	-0.2 to 9	-0.3 to 9.2	V	
			Full range	-0.2 to 3.5		-0.2 to 8.5		V	
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 1 MΩ	25°C	3.2	4.1	8.2	8.9	V	
			-40°C	3.2	4.1	8.2	8.9		
			85°C	3.2	4.2	8.2	8.9		
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C	0	25	0	25	mV	
			-40°C	0	25	0	25		
			85°C	0	25	0	25		
A <sub>VD</sub>	Large-signal differential voltage amplification	R <sub>L</sub> = 1 MΩ, See Note 6	25°C	250	525	500	850	V/mV	
			-40°C	250	900	500	1550		
			85°C	150	300	250	585		
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	70	95	75	97	dB	
			-40°C	70	95	75	97		
			85°C	70	95	75	97		
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 1.4 V	25°C	75	98	75	98	dB	
			-40°C	75	98	75	98		
			85°C	75	98	75	98		
I <sub>DD</sub>	Supply current (two amplifiers)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C	20	34	29	46	μA	
			-40°C	31	54	50	86		
			85°C	15	26	20	36		

† Full range is -40°C to 80°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.



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**electrical characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TLC1079I						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω, R <sub>I</sub> = 1 MΩ	25°C		190	850		200	1150	μV
		Full range			1350			1650	
α <sub>VIO</sub> Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		μV/°C
I <sub>IO</sub> Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> / 2, V <sub>IC</sub> = V <sub>DD</sub> / 2	25°C		0.1	60		0.1	60	pA
		85°C		24	1000		26	1000	
I <sub>IB</sub> Input bias current (see Note 4)		25°C		0.6	60		0.7	60	pA
		85°C		200	2000		220	2000	
V <sub>ICR</sub> Common-mode input voltage range (see Note 5)		25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2		V
		Full range	-0.2 to 3.5			-0.2 to 8.5			V
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
		-40°C	3.2	4.1		8.2	8.9		
		85°C	3.2	4.2		8.2	8.9		
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C		0	25		0	25	mV
		-40°C		0	25		0	25	
		85°C		0	25		0	25	
A <sub>VD</sub> Large-signal differential voltage amplification	R <sub>L</sub> = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
		-40°C	250	900		500	1550		
		85°C	150	330		250	585		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	70	95		75	97		dB
		-40°C	70	95		75	97		
		85°C	70	95		75	97		
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	V <sub>DD</sub> = 5 V to 10 V, V <sub>O</sub> = 1.4 V	25°C	75	98		75	98		dB
		-40°C	75	98		75	98		
		85°C	75	98		75	98		
I <sub>DD</sub> Supply current (four amplifiers)	V <sub>O</sub> = V <sub>DD</sub> / 2, V <sub>IC</sub> = V <sub>DD</sub> / 2, No load	25°C		40	68		57	92	μA
		-40°C		62	108		98	172	
		85°C		29	52		40	72	

† Full range is -40°C to 85°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.  
 5. This range also applies to each input individually.  
 6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.



**TLC1078, TLC1078Y, TLC1079, TLC1079Y**  
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**OPERATIONAL AMPLIFIERS**

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**operating characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TLC1078I						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	R <sub>L</sub> = 1 M $\Omega$ , C <sub>L</sub> = 20 pF, V <sub>I(PP)</sub> = 1 V, See Figure 1	25°C	32			47			V/ms
		-40°C	39			59			
		85°C	25			34			
V <sub>n</sub> Equivalent input noise voltage	f = 1 kHz, R <sub>S</sub> = 20 $\Omega$	25°C	68			68			nV/ $\sqrt{\text{Hz}}$
B <sub>1</sub> Unity-gain bandwidth	C <sub>L</sub> = 20 pF, See Figure 2	25°C	85			110			kHz
		-40°C	130			155			
		85°C	55			80			
$\phi_m$ Phase margin at unity gain	C <sub>L</sub> = 20 pF, See Figure 2	25°C	34°			38°			
		-40°C	38°			40°			
		85°C	28°			32°			

**operating characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TLC1079I						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	R <sub>L</sub> = 1 M $\Omega$ , C <sub>L</sub> = 20 pF, V <sub>I(PP)</sub> = 1 V, See Figure 1	25°C	32			47			V/ms
		-40°C	39			59			
		85°C	25			34			
V <sub>n</sub> Equivalent input noise voltage	f = 1 kHz, R <sub>S</sub> = 20 $\Omega$	25°C	68			68			nV/ $\sqrt{\text{Hz}}$
B <sub>1</sub> Unity-gain bandwidth	C <sub>L</sub> = 20 pF, See Figure 2	25°C	85			110			kHz
		-40°C	130			155			
		85°C	55			80			
$\phi_m$ Phase margin at unity gain	C <sub>L</sub> = 20 pF, See Figure 2	25°C	34°			38°			
		-40°C	38°			42°			
		85°C	28°			32°			



TLC1078, TLC1078Y, TLC1079, TLC1079Y  
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**electrical characteristics at specified operating free-air temperature**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TLC1078M						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 1.4 V, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 $\Omega$ , R <sub>L</sub> = 1 M $\Omega$	25°C	160		450	180		600	$\mu$ V
		Full range	1250			1400			
$\alpha$ V <sub>IO</sub> Temperature coefficient of input offset voltage		25°C to 125°C	1.4			1.4			$\mu$ V/°C
I <sub>IO</sub> Input offset current (see Note 4)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2	25°C	0.1	60		0.1	60		pA
		125°C	1.4	15		1.8	15		nA
I <sub>IB</sub> Input bias current (see Note 4)		25°C	0.6	60		0.7	60		pA
		125°C	9	35		10	35		nA
V <sub>ICR</sub> Common-mode input voltage range (see Note 5)		25°C	0 to 4	-0.3 to 4.2		0 to 9	-0.3 to 9.2		V
		Full range	0 to 3.5			0 to 8.5			V
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 100 mV, R <sub>L</sub> = 1 M $\Omega$	25°C	3.2	4.1		8.2	8.9		V
		-55°C	3.2	4.1		8.2	8.8		
		125°C	3.2	4.2		8.2	9		
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -100 mV, I <sub>OL</sub> = 0	25°C		0	25		0	25	mV
		-55°C		0	25		0	25	
		125°C		0	25		0	25	
A <sub>VD</sub> Large-signal differential voltage amplification	R <sub>L</sub> = 1 M $\Omega$ , See Note 6	25°C	250	525		500	850		V/mV
		-55°C	250	950		500	1750		
		125°C	35	200		75	380		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	70	95		75	97		dB
		-55°C	70	95		75	97		
		125°C	70	85		75	91		
k <sub>SVR</sub> Supply-voltage rejection ratio ( $\Delta$ V <sub>DD</sub> / $\Delta$ V <sub>IO</sub> )	V <sub>O</sub> = 1.4 V	25°C	75	98		75	98		dB
		-55°C	70	98		70	98		
		125°C	70	98		70	98		
I <sub>DD</sub> Supply current (two amplifiers)	V <sub>O</sub> = V <sub>DD</sub> /2, V <sub>IC</sub> = V <sub>DD</sub> /2, No load	25°C		20	34		29	46	$\mu$ A
		-55°C		35	60		56	96	
		125°C		14	24		18	30	

† Full range is -55°C to 125°C.

- NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.  
5. This range also applies to each input individually.  
6. At V<sub>DD</sub> = 5 V, V<sub>O</sub> = 0.25 V to 2 V; at V<sub>DD</sub> = 10 V, V<sub>O</sub> = 1 V to 6 V.

**TLC1078, TLC1078Y, TLC1079, TLC1079Y**  
**LinCMOS™  $\mu$ POWER PRECISION**  
**OPERATIONAL AMPLIFIERS**

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**electrical characteristics at specified free-air temperature**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLC1079M						UNIT
			$V_{DD} = 5\text{ V}$			$V_{DD} = 10\text{ V}$			
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 1.4\text{ V}, V_{IC} = 0,$ $R_S = 50\ \Omega, R_I = 1\text{ M}\Omega$	25°C	190 850		200 1150		$\mu\text{V}$		
Full range		1600		1900					
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25°C to 125°C	1.4		1.4		$\mu\text{V}/^\circ\text{C}$		
$I_{IO}$ Input offset current (see Note 4)	$V_O = V_{DD}/2,$ $V_{IC} = V_{DD}/2$	25°C	0.1	60	0.1	60	pA		
		125°C	1.4	15	1.8	15	nA		
$I_{IB}$ Input bias current (see Note 4)		25°C	0.6	60	0.7	60	pA		
		125°C	9	35	10	35	nA		
$V_{ICR}$ Common mode input voltage range (see Note 5)		25°C	0 to 4	-0.3 to 4.2	0 to 9	-0.3 to 9.2	V		
	Full range		0 to 3.5		0 to 8.5		V		
$V_{OH}$ High-level output voltage	$V_{ID} = 100\text{ mV},$ $R_L = 1\text{ M}\Omega$	25°C	3.2	4.1	8.2	8.9	V		
		-55°C	3.2	4.1	8.2	8.9			
		125°C	3.2	4.2	8.2	9			
$V_{OL}$ Low-level output voltage	$V_{ID} = -100\text{ mV},$ $I_{OL} = 0$	25°C	0 25		0 25		mV		
		-55°C	0 25		0 25				
		125°C	0 25		0 25				
$A_{VD}$ Large-signal differential voltage amplification	$R_L = 1\text{ M}\Omega,$ See Note 6	25°C	250	525	500	850	V/mV		
		-55°C	250	950	500	1750			
		125°C	35	200	75	380			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	25°C	70	95	75	97	dB		
		-55°C	70	95	75	97			
		125°C	70	85	75	91			
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 5\text{ V to }10\text{ V},$ $V_O = 1.4\text{ V}$	25°C	75	98	75	98	dB		
		-55°C	70	98	70	98			
		125°C	70	98	70	98			
$I_{DD}$ Supply current (four amplifiers)	$V_O = V_{DD}/2,$ $V_{IC} = V_{DD}/2,$ No load	25°C	40	68	57	92	$\mu\text{A}$		
		-55°C	69	120	111	192			
		125°C	27	48	35	60			

† Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At  $V_{DD} = 5\text{ V}, V_O = 0.25\text{ V to }2\text{ V};$  at  $V_{DD} = 10\text{ V}, V_O = 1\text{ V to }6\text{ V}.$



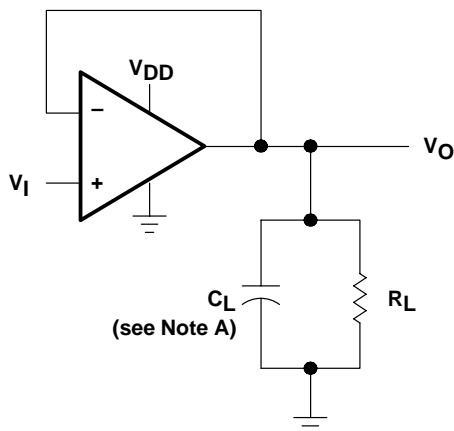
operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TLC1078M						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	R <sub>L</sub> = 1 M $\Omega$ , C <sub>L</sub> = 20 pF, V <sub>I(PP)</sub> = 1 V, See Figure 1	25°C		32			47	V/ms	
		-55°C		41			63		
		125°C		20			27		
V <sub>n</sub> Equivalent input noise voltage	f = 1 kHz, R <sub>S</sub> = 20 $\Omega$	25°C		68			68	nV/ $\sqrt{\text{Hz}}$	
B <sub>1</sub> Unity-gain bandwidth	C <sub>L</sub> = 20 pF, See Figure 2	25°C		85			110	kHz	
		-55°C		140			165		
		125°C		45			70		
$\phi_m$ Phase margin at unity gain	C <sub>L</sub> = 20 pF, See Figure 2	25°C		34°			38°		
		-55°C		39°			43°		
		125°C		25°			29°		

operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TLC1079M						UNIT
			V <sub>DD</sub> = 5 V			V <sub>DD</sub> = 10 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	R <sub>L</sub> = 1 M $\Omega$ , C <sub>L</sub> = 20 pF, V <sub>I(PP)</sub> = 1 V, See Figure 1	25°C		32			47	V/ms	
		-55°C		41			63		
		125°C		20			27		
V <sub>n</sub> Equivalent input noise voltage	f = 1 kHz, R <sub>S</sub> = 20 $\Omega$	25°C		68			68	nV/ $\sqrt{\text{Hz}}$	
B <sub>1</sub> Unity-gain bandwidth	C <sub>L</sub> = 20 pF, See Figure 2	25°C		85			110	kHz	
		-55°C		140			165		
		125°C		45			70		
		25°C		34°			38°		
$\phi_m$ Phase margin at unity gain	C <sub>L</sub> = 20 pF, See Figure 2	-55°C		39°			43°		
		125°C		25°			29°		

PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

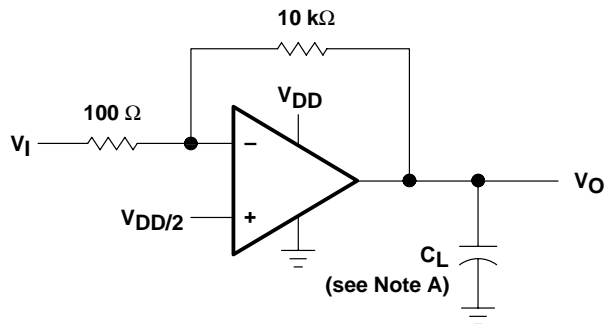


Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	Distribution 3 – 6
$I_{IB}$	Input bias current	vs Free-air temperature 7
$I_{IQ}$	Input offset current	vs Free-air temperature 7
$V_{IC}$	Common-mode input voltage	vs Supply voltage 8
$V_{OH}$	High-level output voltage	vs High-level output current 9, 10
		vs Supply voltage 11
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$V_{OL}$	Low-level output voltage	vs Common-mode input voltage 13, 14
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$A_{VD}$	Large-signal differential voltage amplification	vs Free-air temperature 20
		vs Frequency 21, 22
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$V_{OM}$	Maximum peak output voltage	vs Frequency 23
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$I_{DD}$	Supply current	vs Supply voltage 24
		vs Free-air temperature 25
SR	Slew rate	vs Supply voltage 26
		vs Free-air temperature 27
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$V_n$	Equivalent input noise voltage	vs Frequency 29
$B_1$	Unity-gain bandwidth	vs Supply voltage 30
		vs Free-air temperature 31
$\phi_m$	Phase margin	vs Supply voltage 32
		vs Free-air temperature 33
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	Phase shift	vs Frequency 21, 22



TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC1078  
 INPUT OFFSET VOLTAGE  
 TEMPERATURE COEFFICIENT

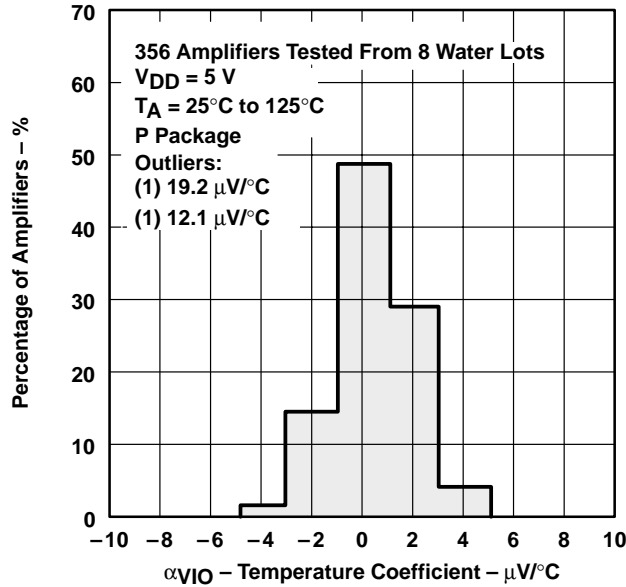


Figure 3

DISTRIBUTION OF TLC1078  
 INPUT OFFSET VOLTAGE  
 TEMPERATURE COEFFICIENT

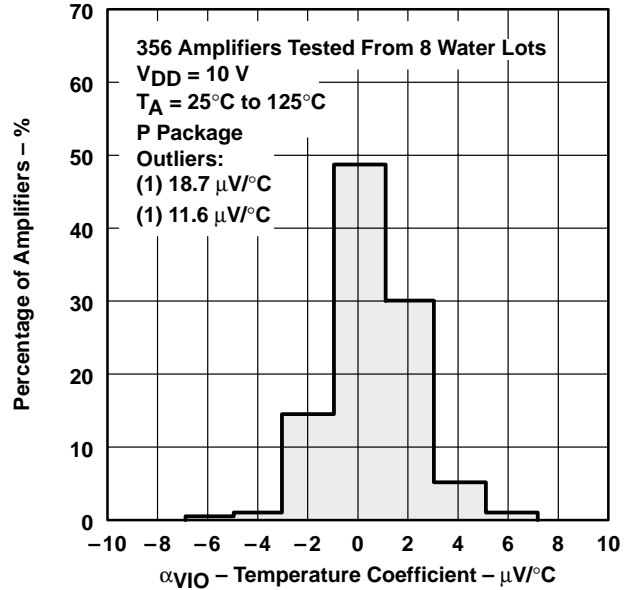


Figure 4

DISTRIBUTION OF TLC1079  
 INPUT OFFSET VOLTAGE  
 TEMPERATURE COEFFICIENT

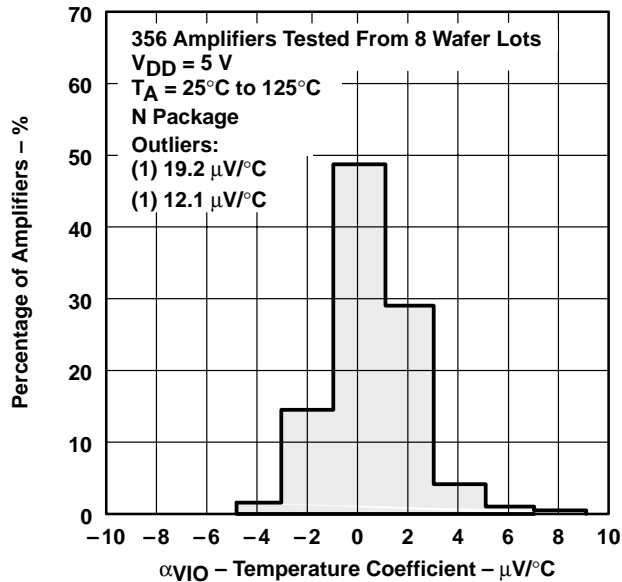


Figure 5

DISTRIBUTION OF TLC1079  
 INPUT OFFSET VOLTAGE  
 TEMPERATURE COEFFICIENT

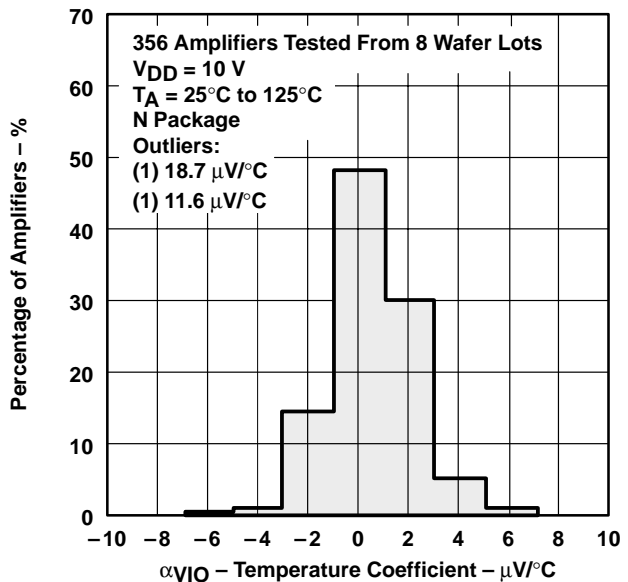
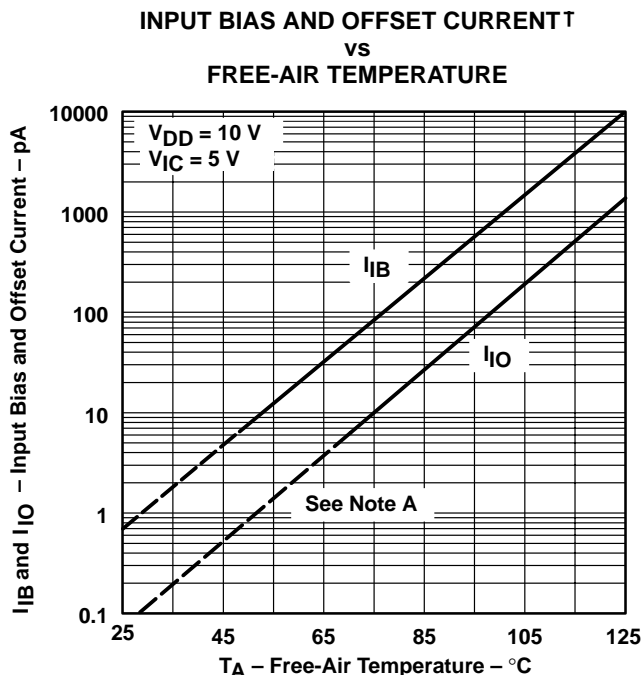


Figure 6

TYPICAL CHARACTERISTICS



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 7

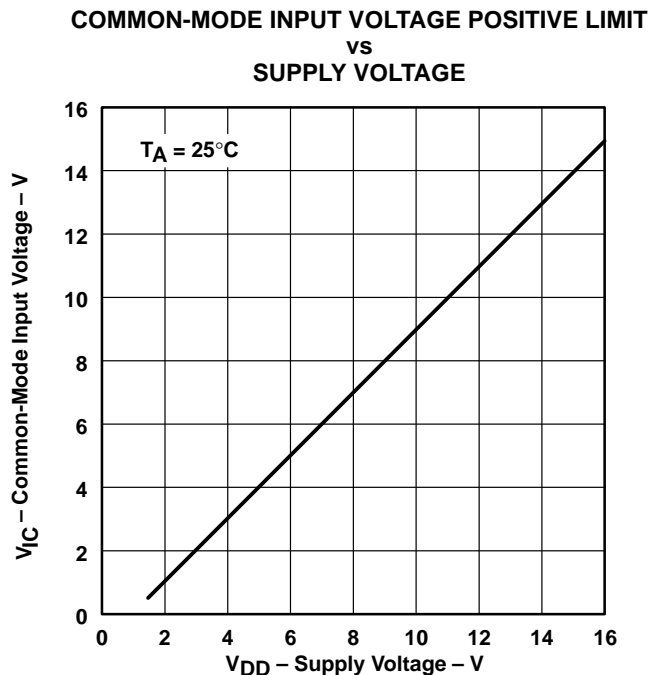


Figure 8

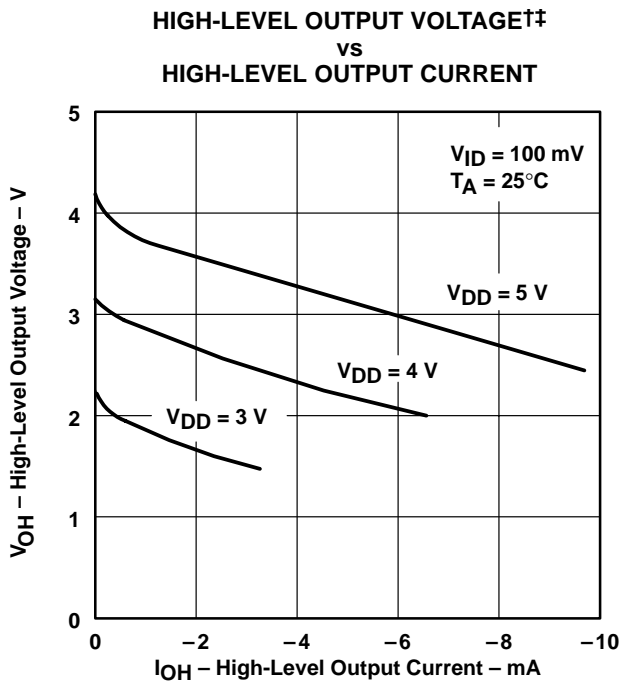


Figure 9

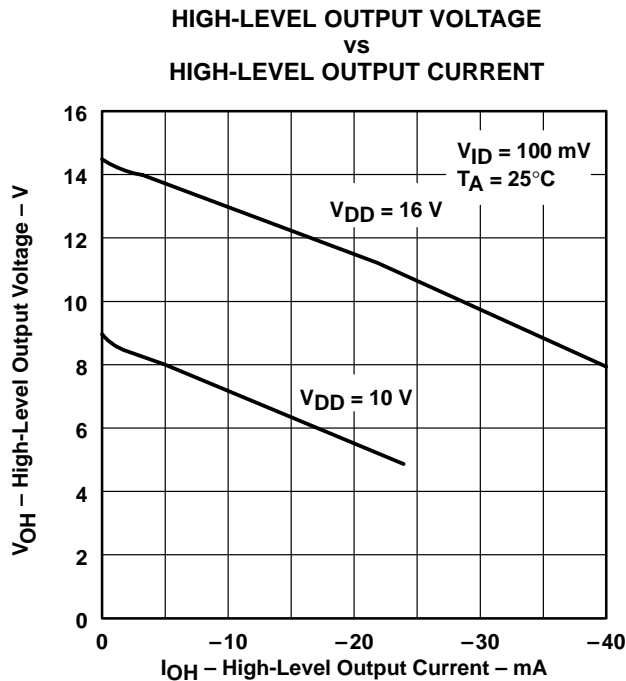


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.  
 ‡ The  $V_{DD} = 3$  V curve does not apply to the TLC107xM.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE  
 vs  
 SUPPLY VOLTAGE

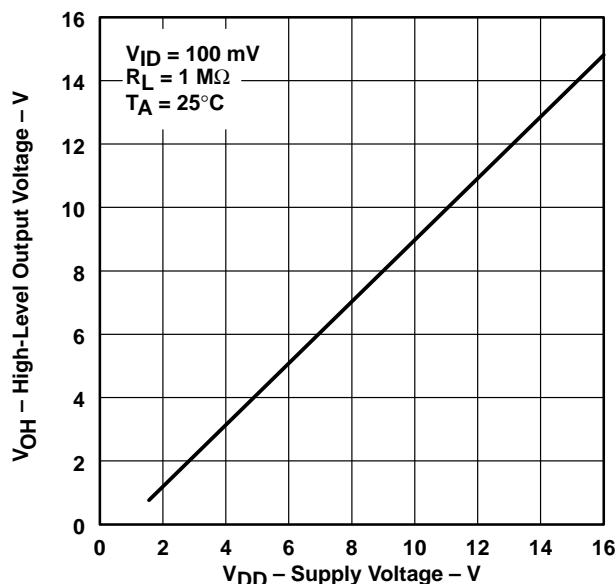


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE†  
 vs  
 FREE-AIR TEMPERATURE

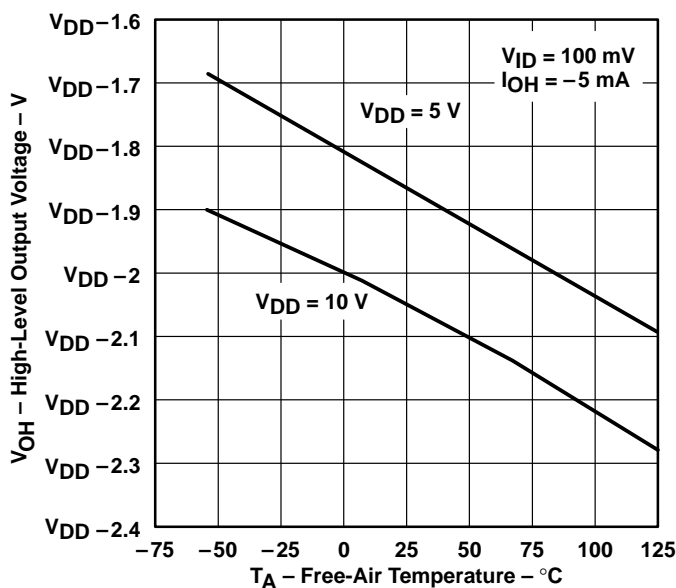


Figure 12

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 COMMON-MODE INPUT VOLTAGE

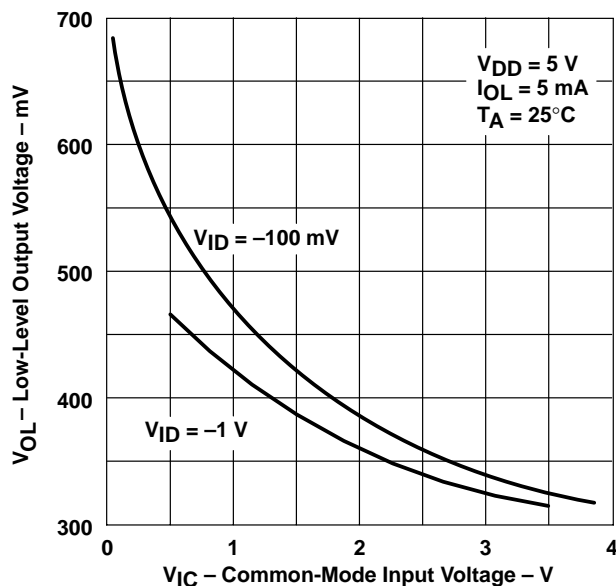


Figure 13

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 COMMON-MODE INPUT VOLTAGE

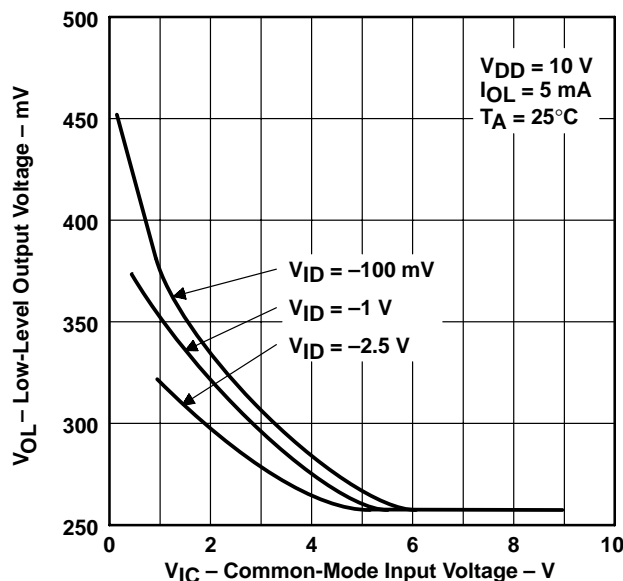


Figure 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 DIFFERENTIAL INPUT VOLTAGE

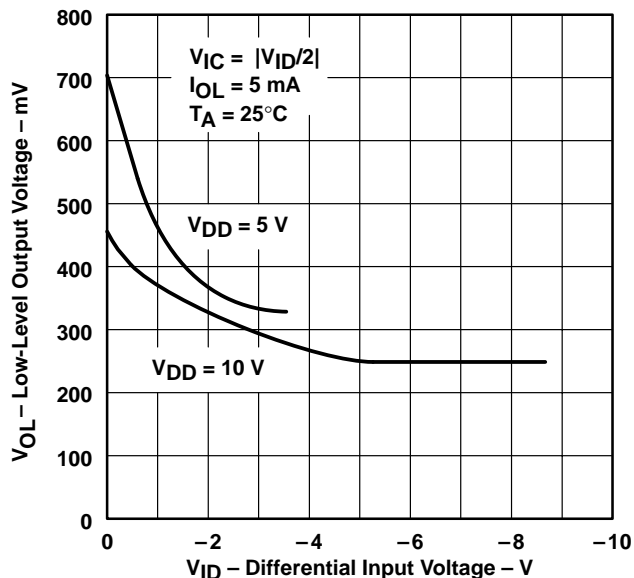


Figure 15

LOW-LEVEL OUTPUT VOLTAGE†  
 vs  
 FREE-AIR TEMPERATURE

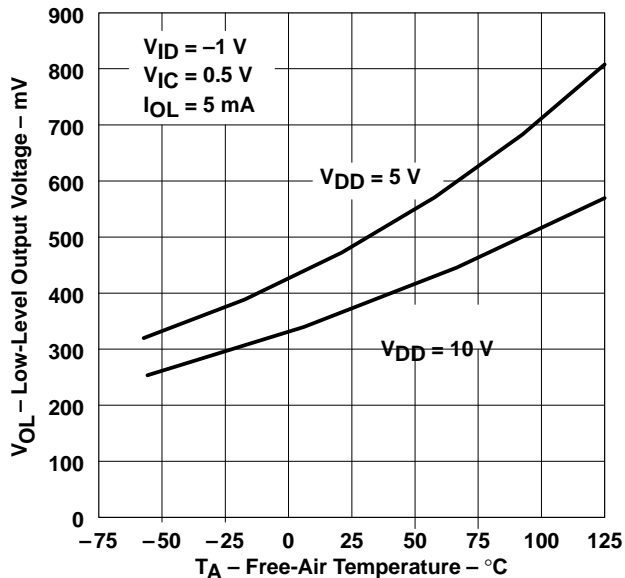


Figure 16

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

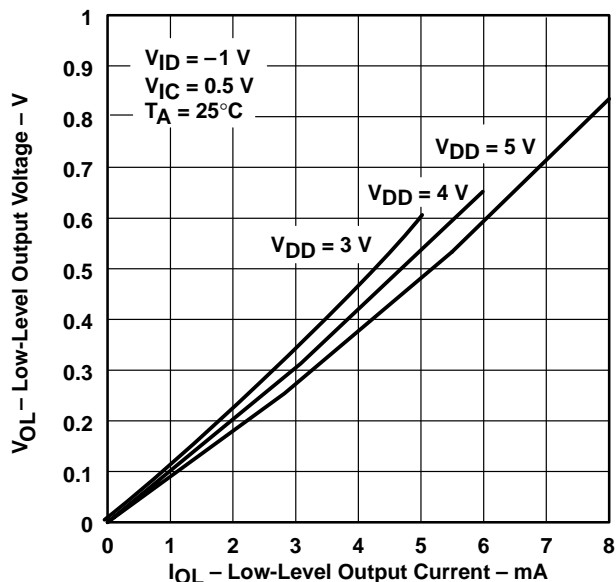


Figure 17

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

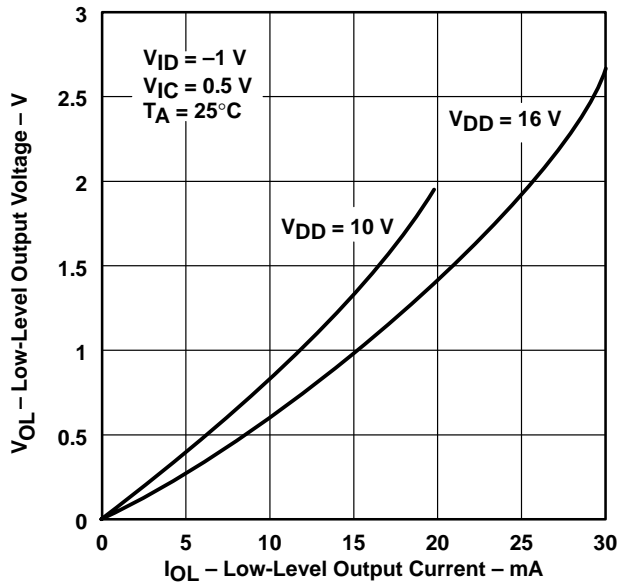


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

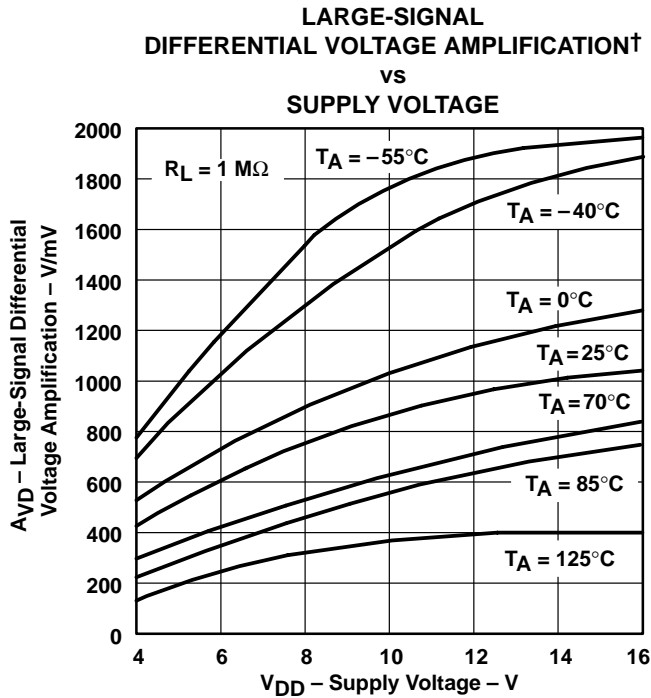


Figure 19

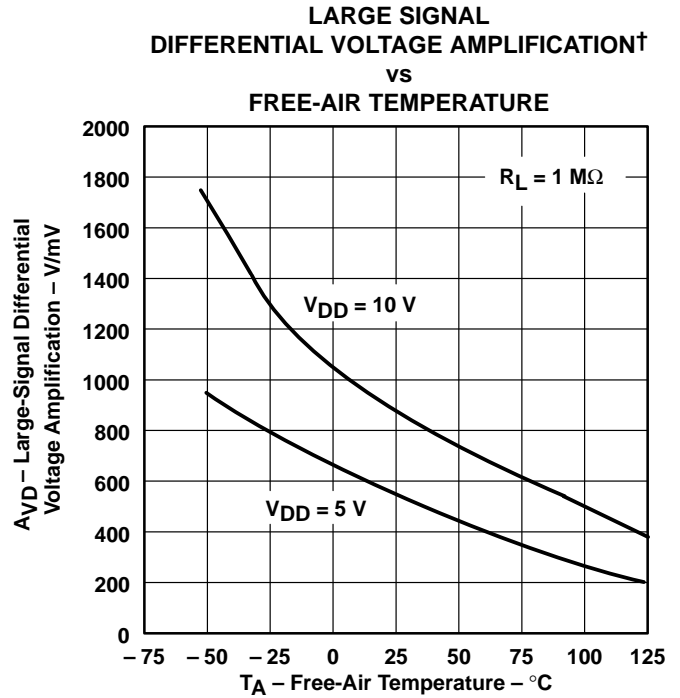


Figure 20

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
AMPLIFICATION AND PHASE SHIFT  
vs  
FREQUENCY**

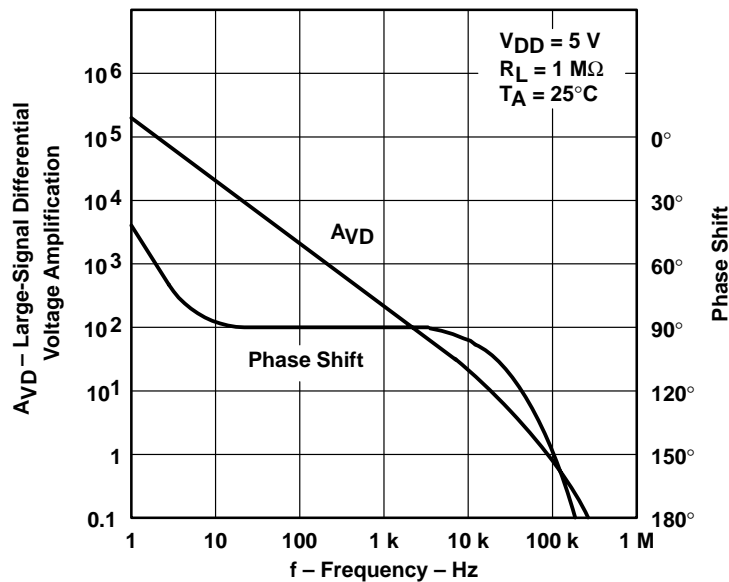


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE SHIFT  
 VS  
 FREQUENCY

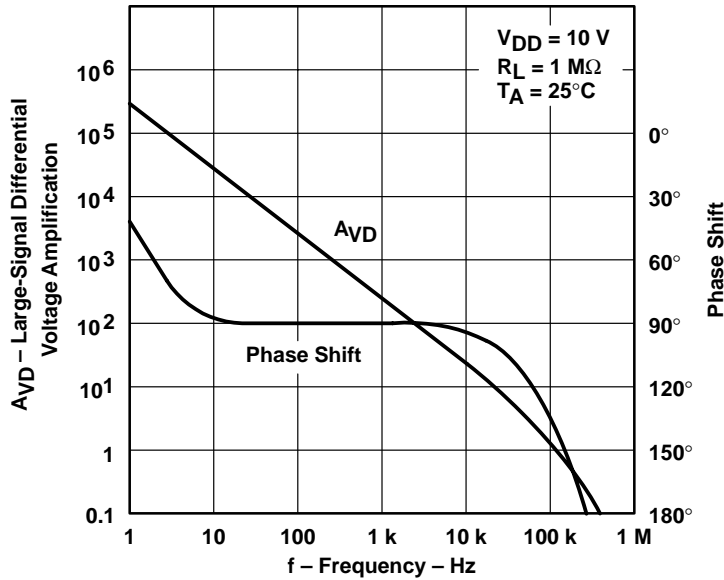


Figure 22

MAXIMUM PEAK OUTPUT VOLTAGE  
 VS  
 FREQUENCY

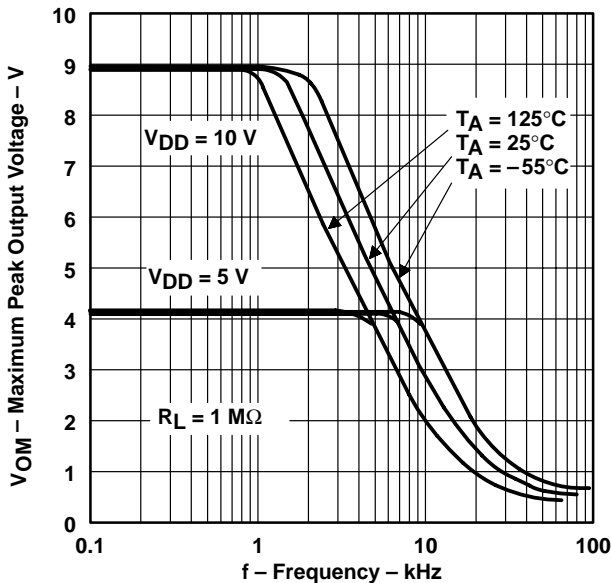


Figure 23

SUPPLY CURRENT†  
 VS  
 SUPPLY VOLTAGE

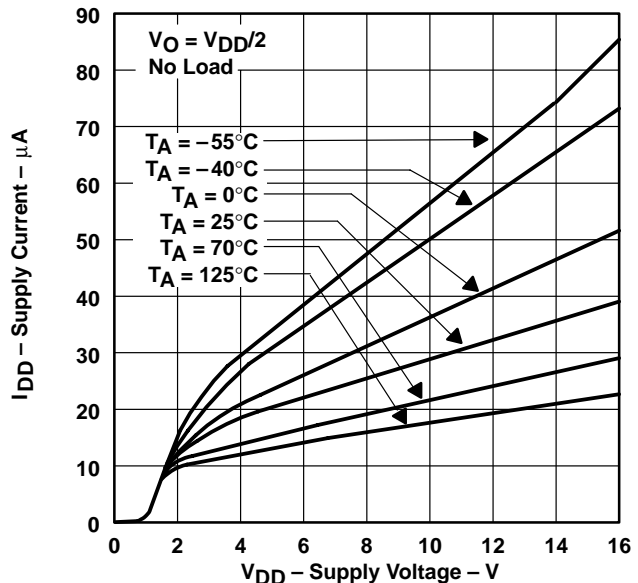
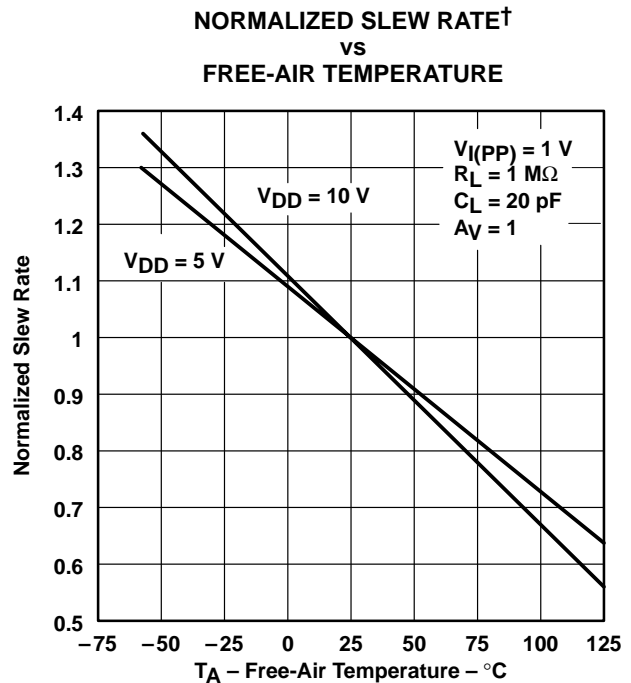
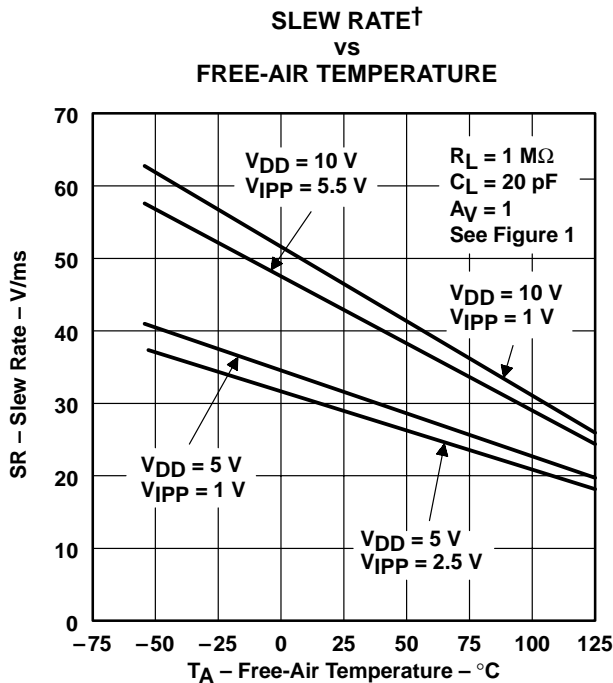
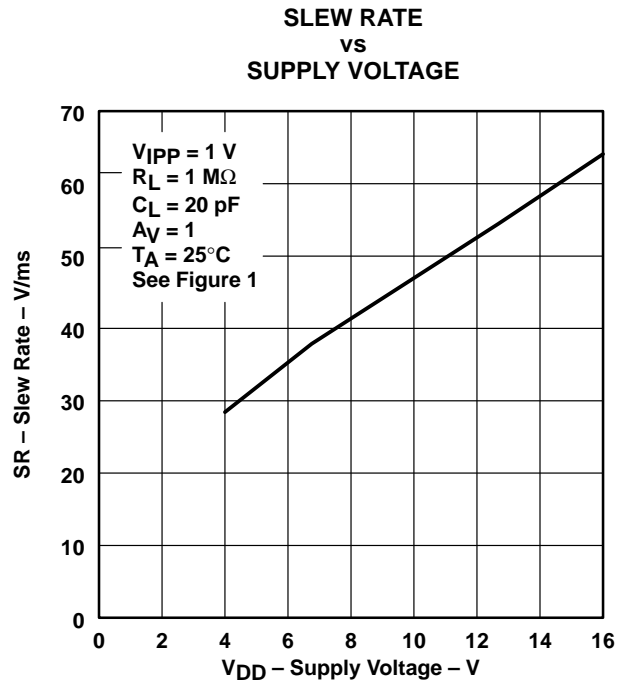
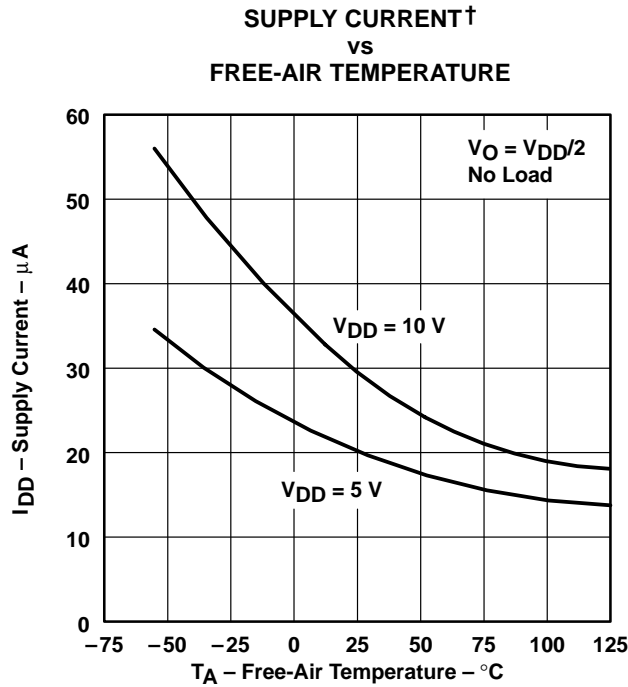


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE  
 VS  
 FREQUENCY

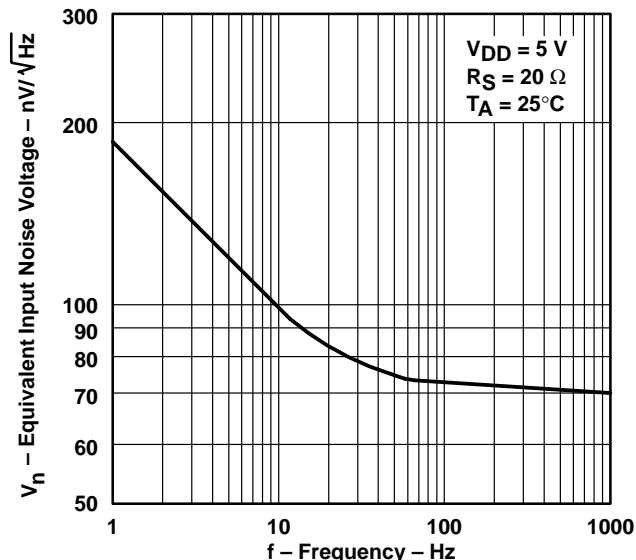


Figure 29

UNITY-GAIN BANDWIDTH  
 VS  
 SUPPLY VOLTAGE

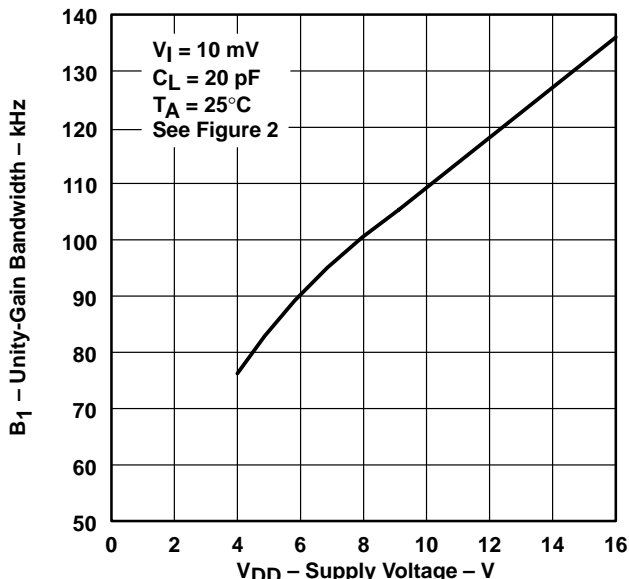


Figure 30

UNITY-GAIN BANDWIDTH†  
 VS  
 FREE-AIR TEMPERATURE

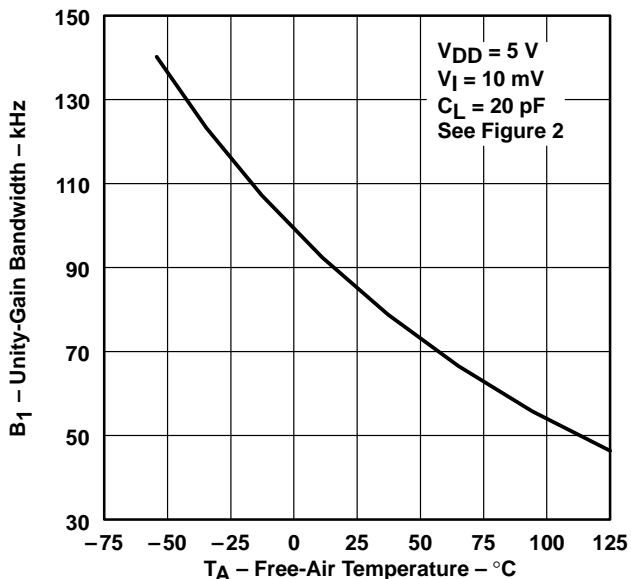


Figure 31

PHASE MARGIN  
 VS  
 SUPPLY VOLTAGE

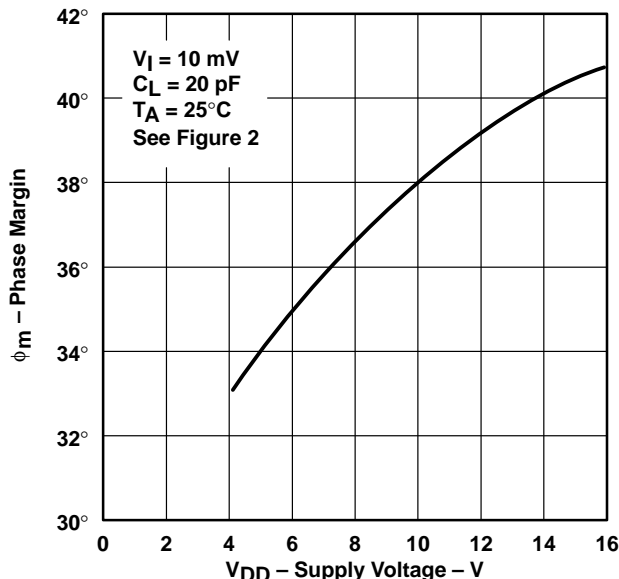


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS

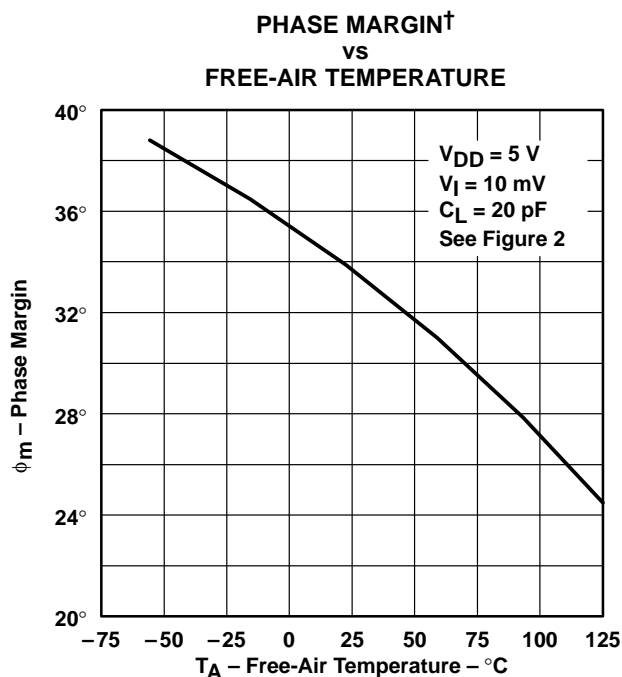


Figure 33

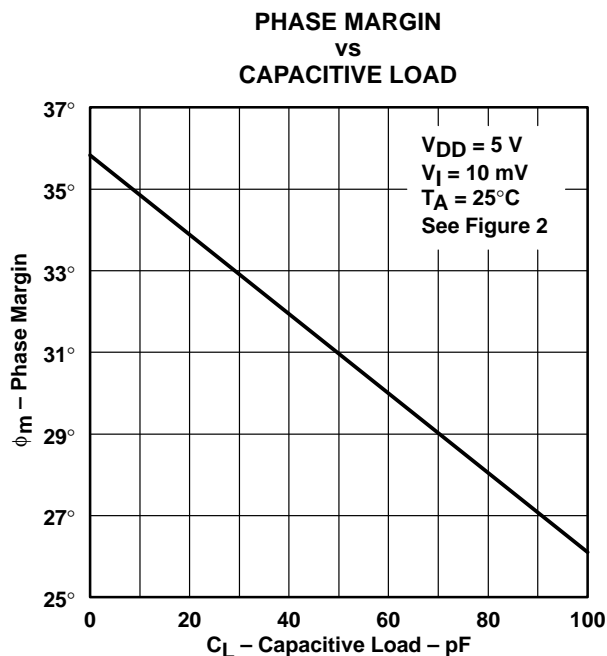


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TLC1078, TLC1078Y, TLC1079, TLC1079Y**  
**LinCMOS™ μPOWER PRECISION**  
**OPERATIONAL AMPLIFIERS**

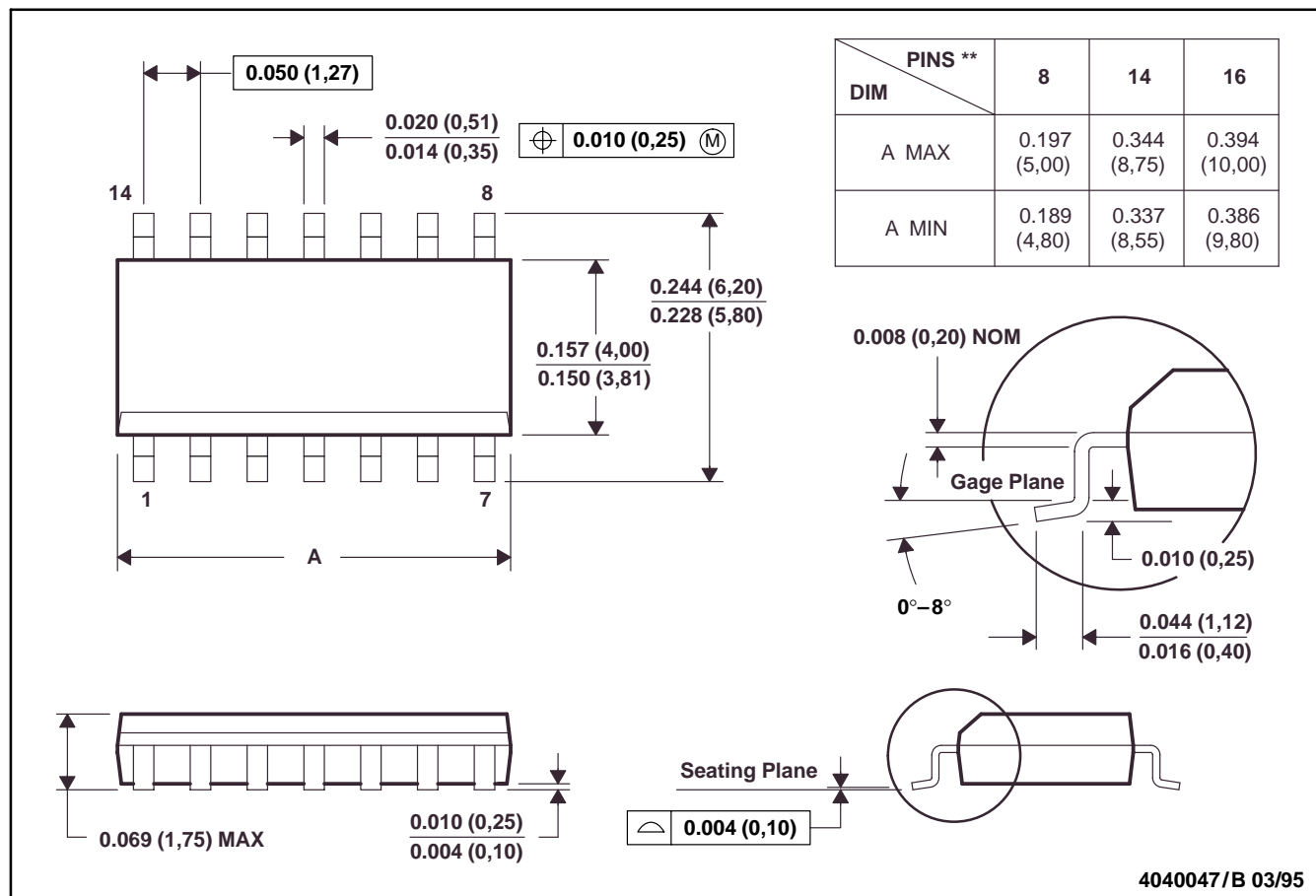
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**MECHANICAL INFORMATION**

**D (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



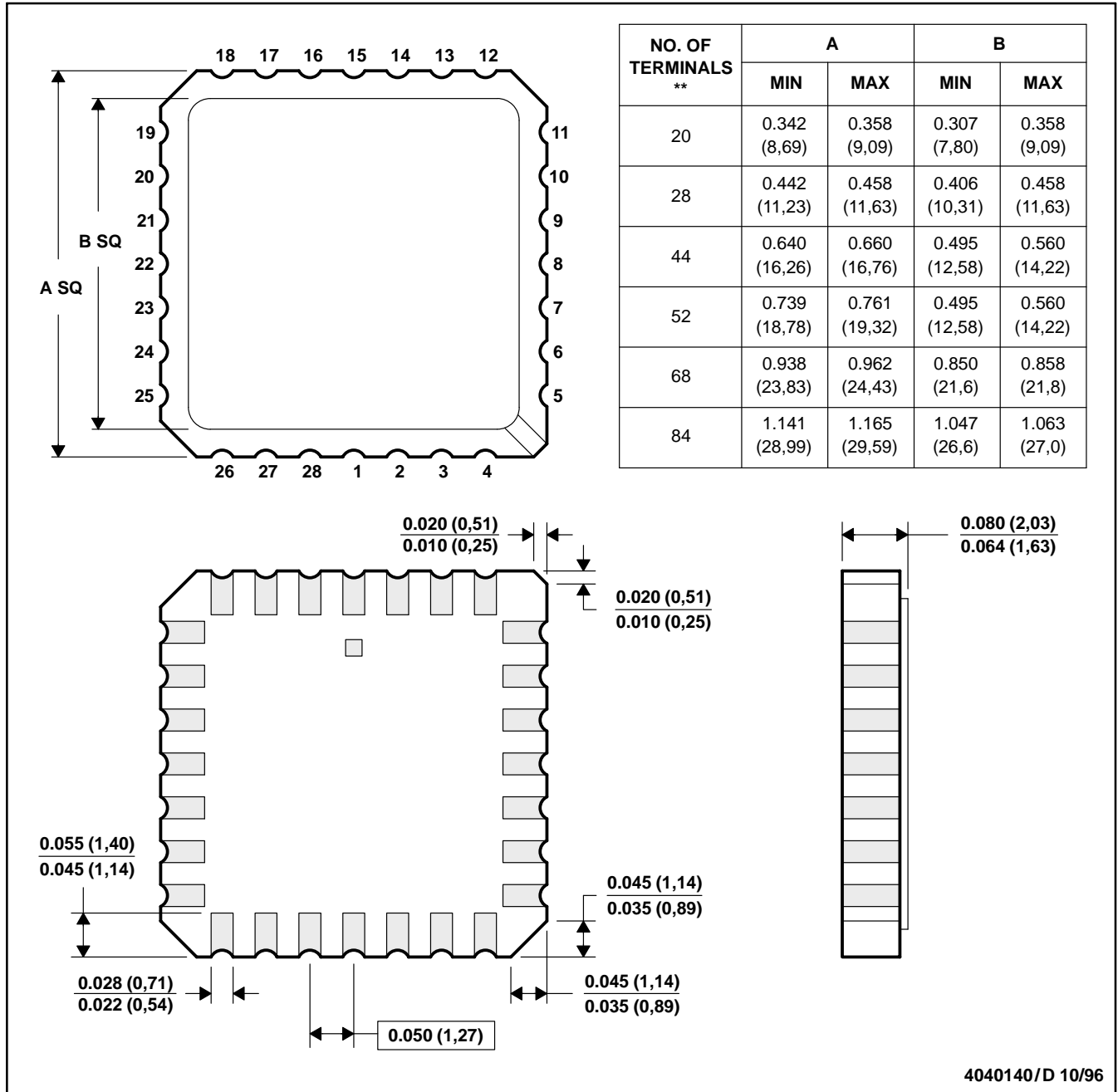
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Four center pins are connected to die mount pad.  
 E. Falls within JEDEC MS-012

MECHANICAL INFORMATION

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a metal lid.  
 D. The terminals are gold plated.  
 E. Falls within JEDEC MS-004

**TLC1078, TLC1078Y, TLC1079, TLC1079Y**  
**LinCMOS™  $\mu$ POWER PRECISION**  
**OPERATIONAL AMPLIFIERS**

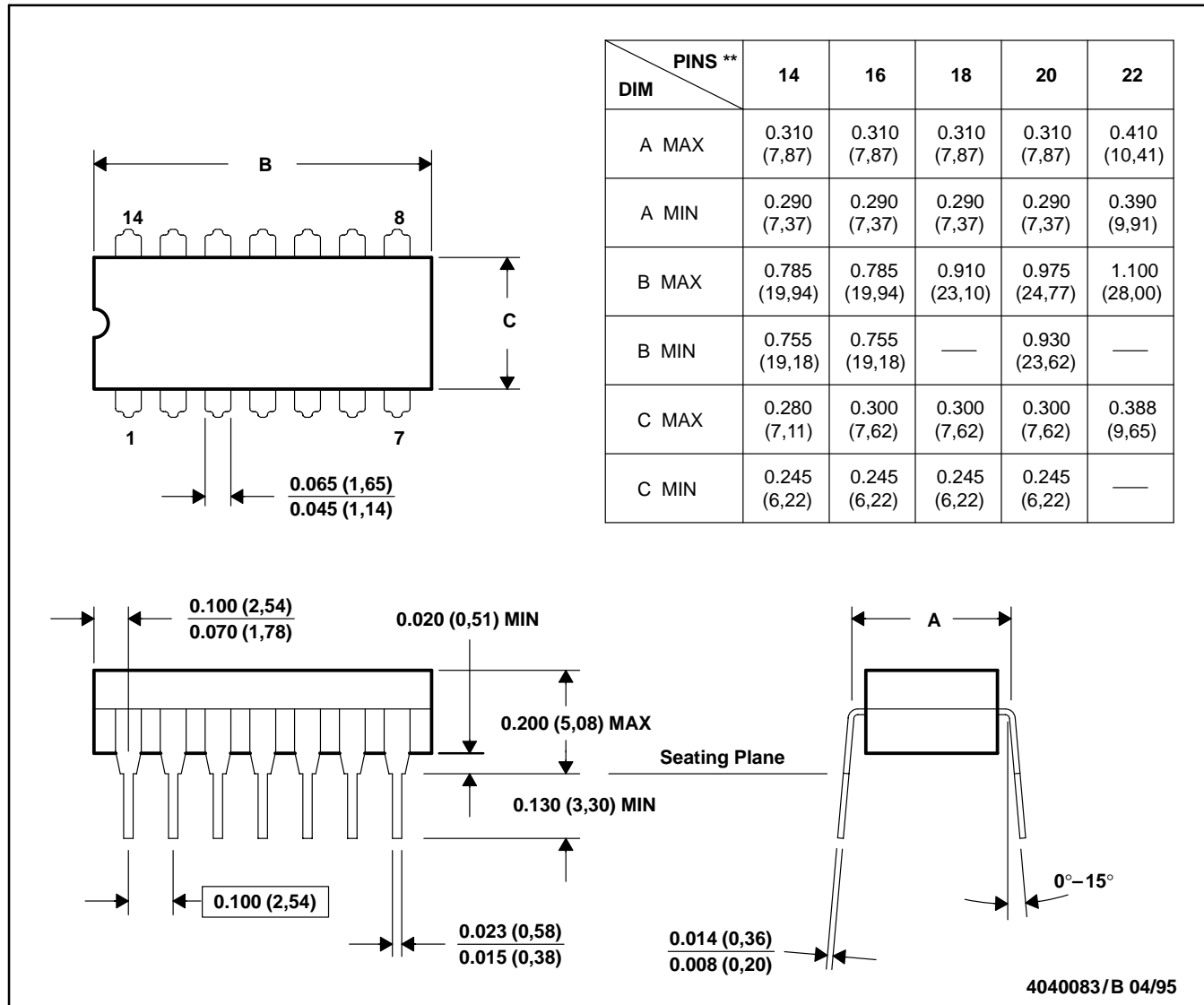
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**MECHANICAL INFORMATION**

**J (R-GDIP-T\*\*)**

**CERAMIC DUAL-IN-LINE PACKAGE**

14 PIN SHOWN

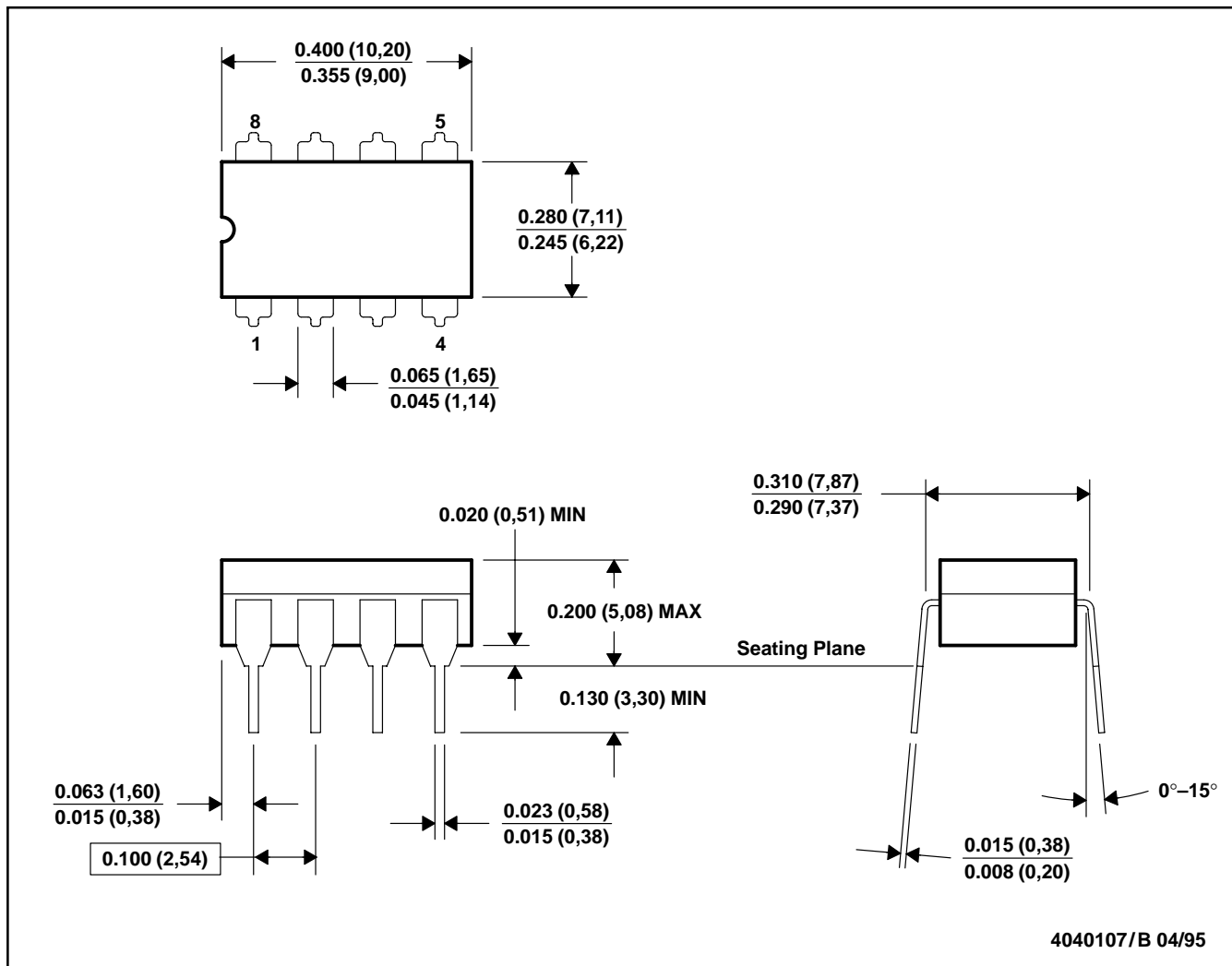


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22

MECHANICAL INFORMATION

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification and/or on pressed ceramic glass frit seal  
 E. Falls within MIL-STD-1835 GDIP1-T8

**TLC1078, TLC1078Y, TLC1079, TLC1079Y**  
**LinCMOS™ μPOWER PRECISION**  
**OPERATIONAL AMPLIFIERS**

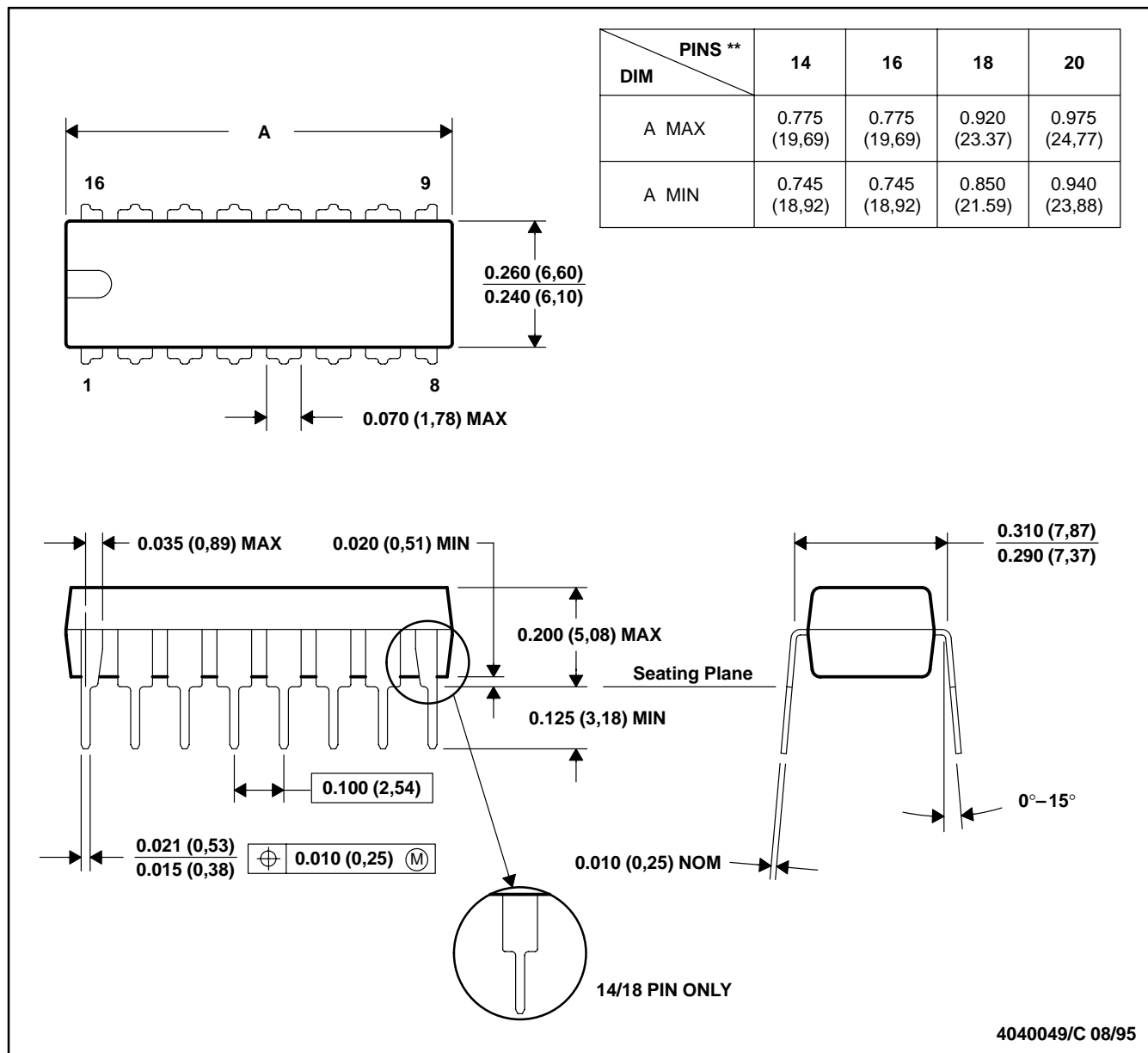
SLOS179A – FEBRUARY 1997 – REVISED MARCH 2001

**MECHANICAL INFORMATION**

**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

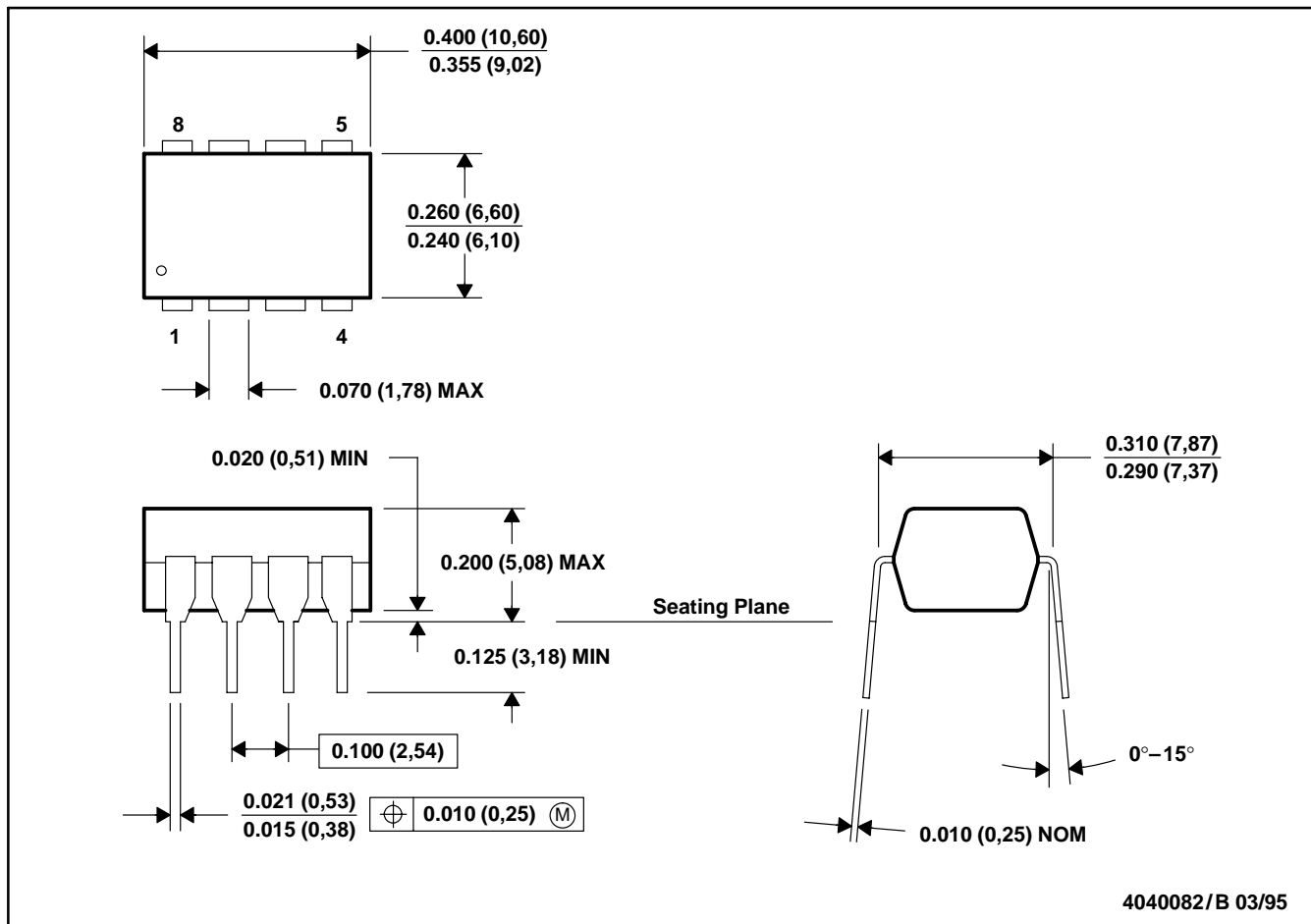


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLC1078CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1078CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1078CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1078CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1078CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC1078CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC1078ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1078IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1078IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1078IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1078IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC1078IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC1078MD	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC1078MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1079CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC1079CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC1079CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC1079CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC1079CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC1079CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC1079CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1079CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1079ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC1079IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC1079IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLC1079IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLC1079IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC1079INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC1078CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC1078IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC1079CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC1079CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC1079IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC1078CDR	SOIC	D	8	2500	346.0	346.0	29.0
TLC1078IDR	SOIC	D	8	2500	346.0	346.0	29.0
TLC1079CDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC1079CNSR	SO	NS	14	2000	346.0	346.0	33.0
TLC1079IDR	SOIC	D	14	2500	346.0	346.0	33.0

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

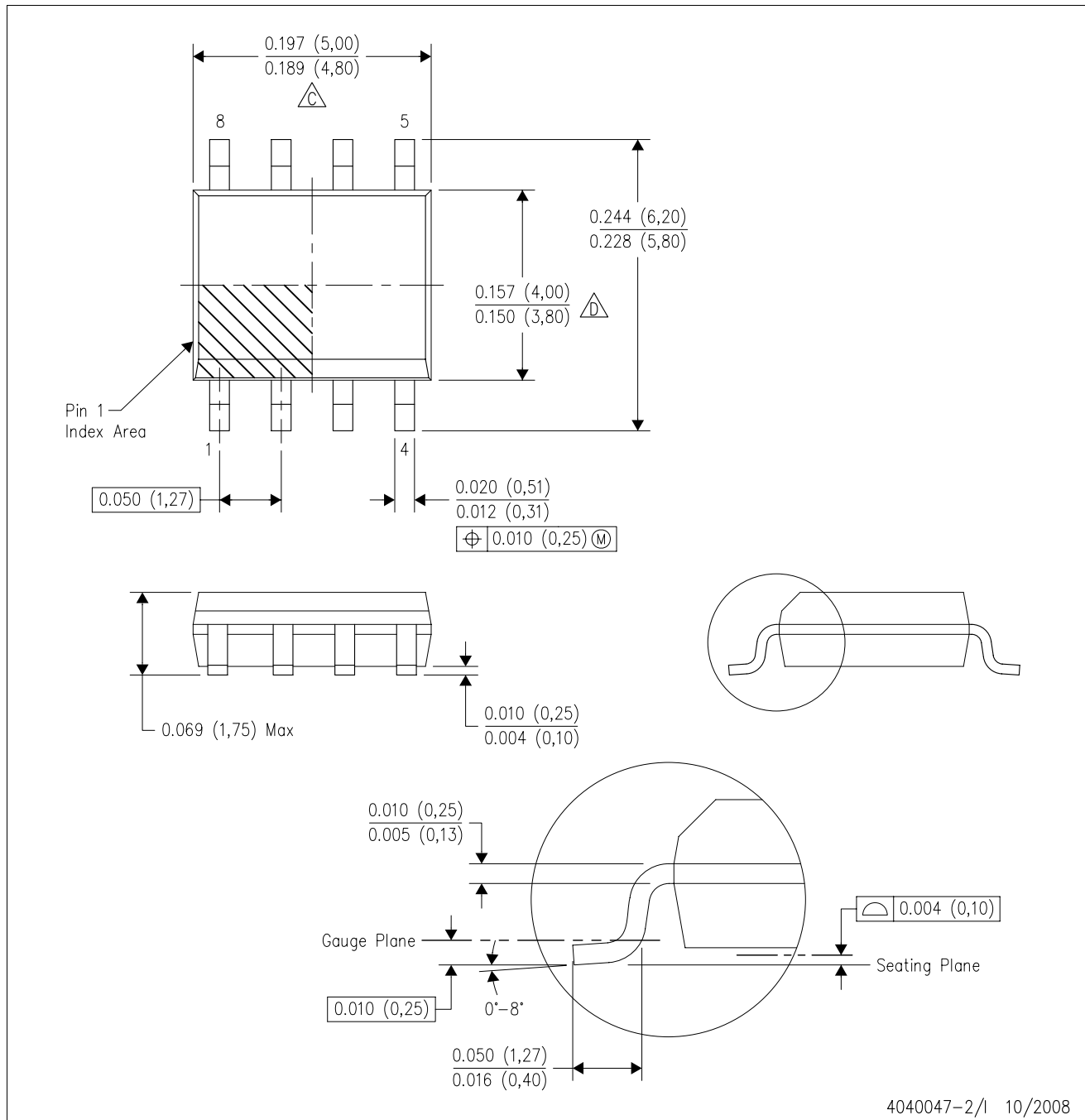
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G8)

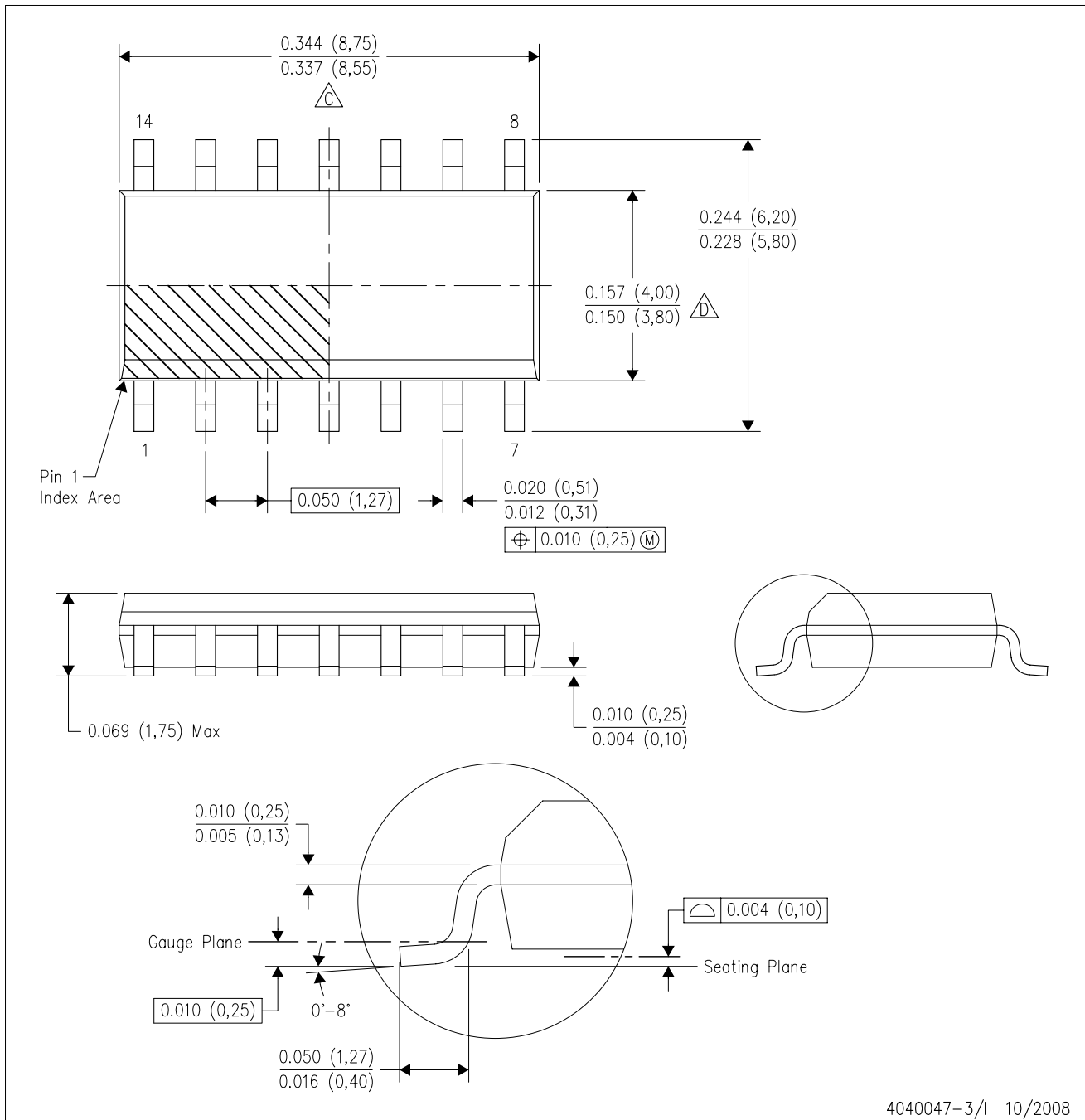
PLASTIC SMALL-OUTLINE PACKAGE





NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.  
 E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  -  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002



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